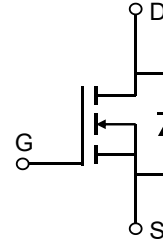


Description

Features

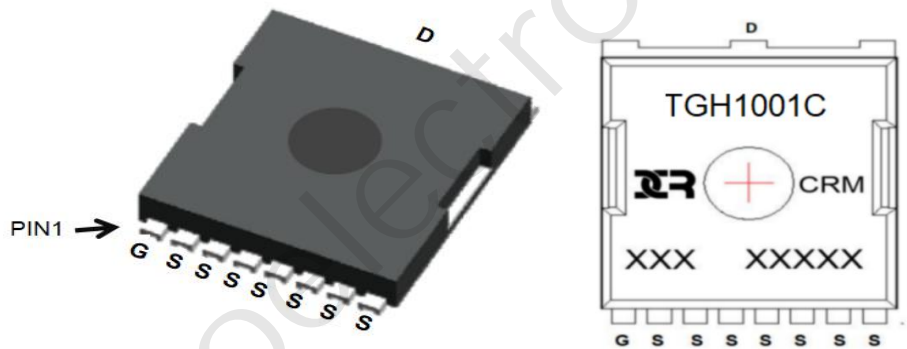
- 100V, 430A
 $R_{DS(ON)}$ Typ = 1.07mΩ @ $V_{GS} = 10V$
 Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS TESTED!
- 100% ΔV_{ds} TESTED!



Schematic Diagram

Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMTGH1001C	CRMTGH1001C	TOLL	TAPING	13"	2000	10000

Absolute Maximum Ratings (@ $T_J = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	430
		$T_C = 100^\circ C$	258
I_{DM}	Pulsed Drain Current ⁽¹⁾	1720	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	1106	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	463
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.27	°C/W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.4	3	3.6	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	1.07	1.4	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 50\text{V},$ $f = 100\text{KHz}$	-	9080	-	pF
C_{oss}	Output Capacitance		-	3509	-	pF
C_{rss}	Reverse Transfer Capacitance		-	79	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 50\text{V}, I_D = 100\text{A}$	-	160	-	nC
Q_{gs}	Gate Source Charge		-	55	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	38	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 50\text{V}$ $I_D = 100\text{A}, R_{GEN} = 3\Omega$	-	30	-	ns
t_r	Turn-On Rise Time		-	80	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	82	-	ns
t_f	Turn-Off Fall Time		-	95	-	ns

Drain-Source Diode Characteristics and Max Ratings

I_S	Maximum Continuous Drain to Source Diode Forward Current	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	430	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	1720	A
V_{SD}	Drain to Source Diode Forward Voltage		-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time		-	85	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	180	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_G = 10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$, $I_{AS} = 66.5\text{A}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

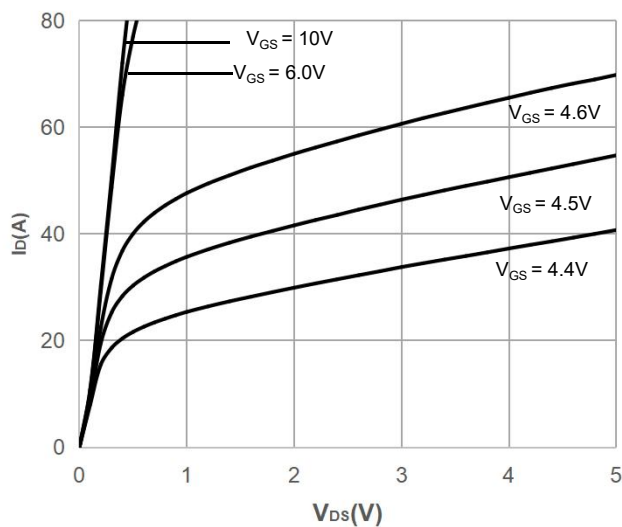


Figure 2: Typical Transfer Characteristics

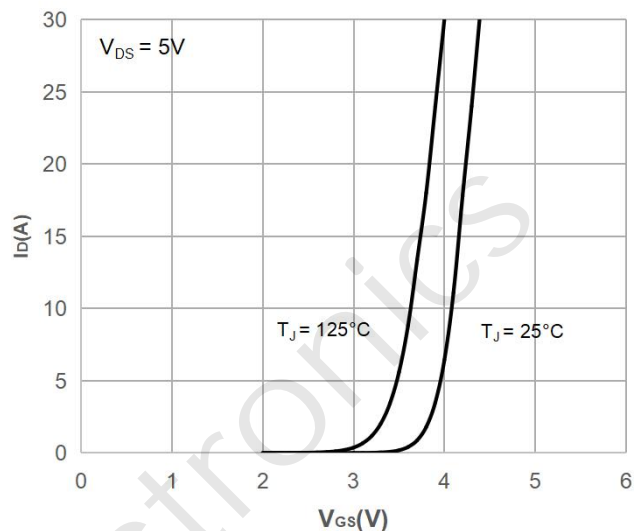


Figure 3: On-resistance vs. Drain Current

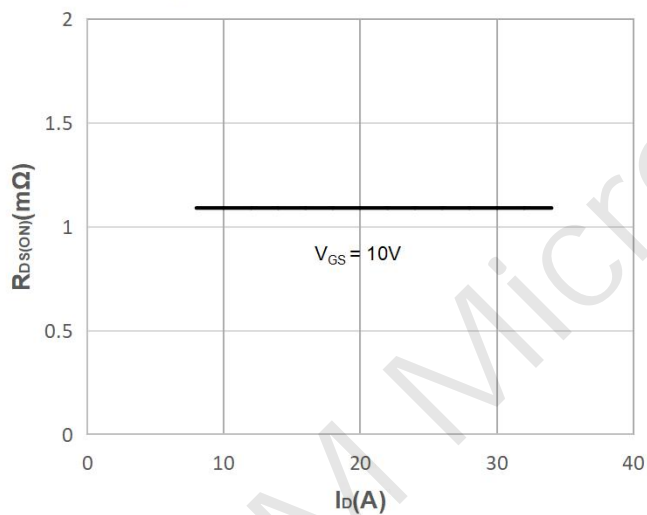


Figure 4: Body Diode Characteristics

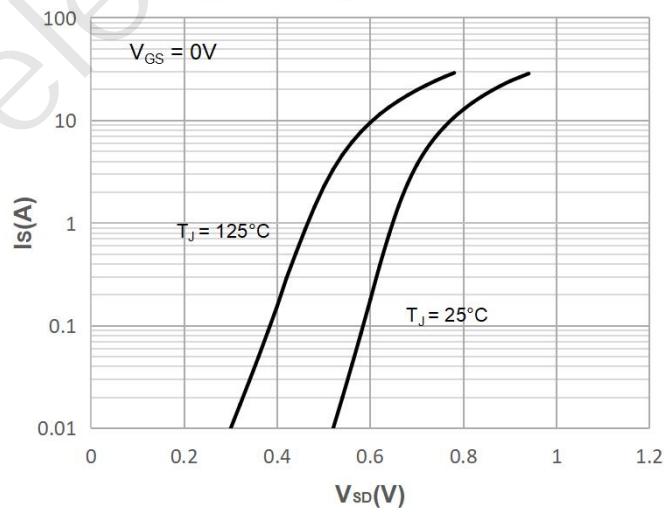


Figure 5: Gate Charge Characteristics

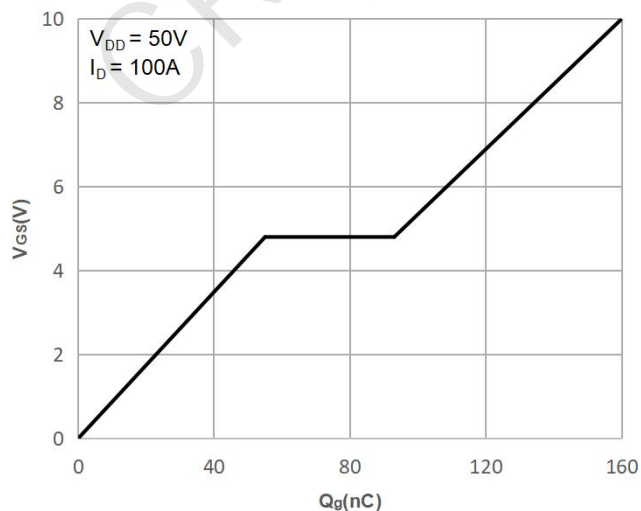
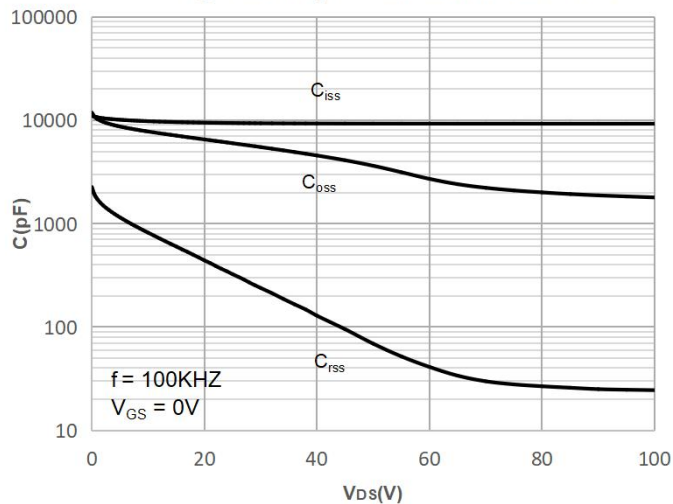


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

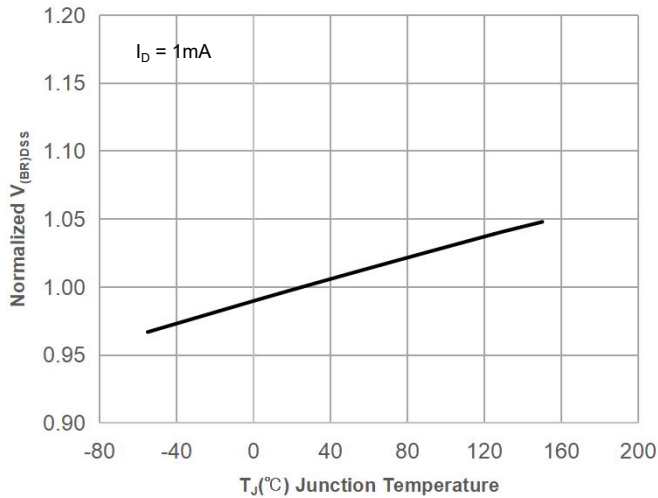


Figure 8: Normalized on Resistance vs. Junction Temperature

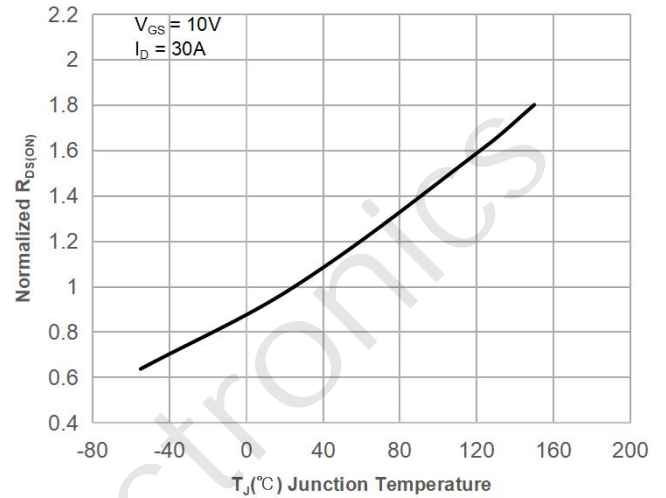


Figure 9: Maximum Safe Operating Area

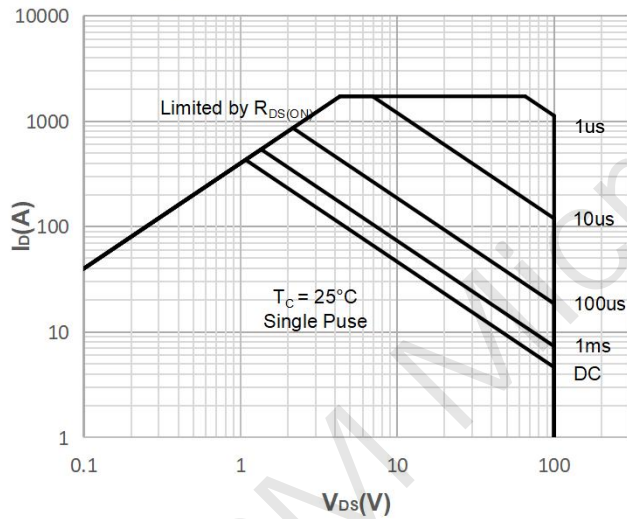


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

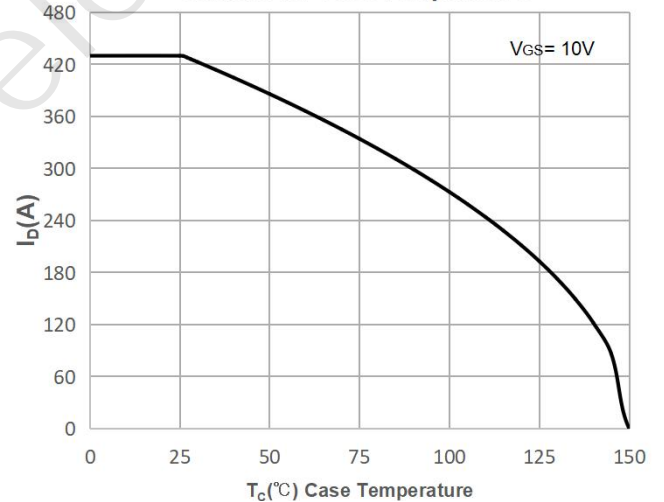


Figure 11: Normalized Maximum Transient Thermal Impedance

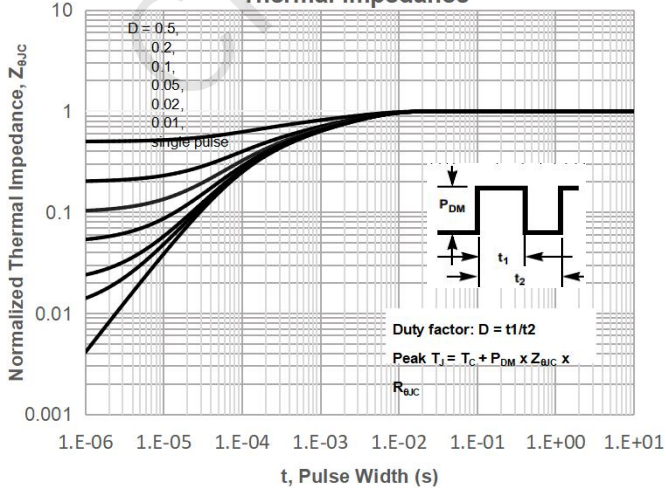
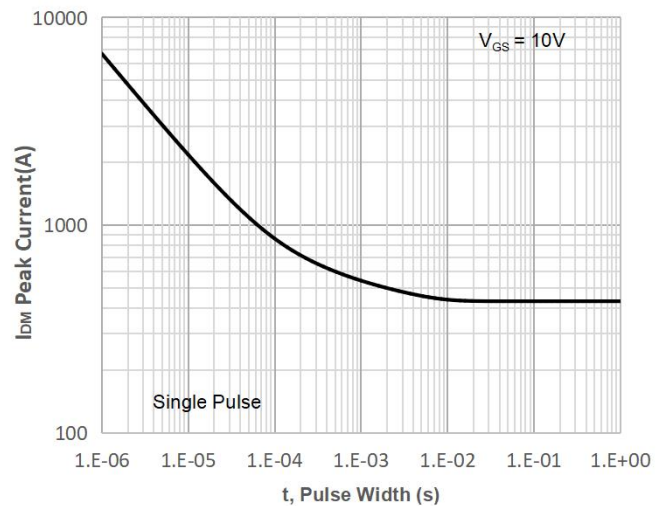


Figure 12: Peak Current Capacity



Test Circuit

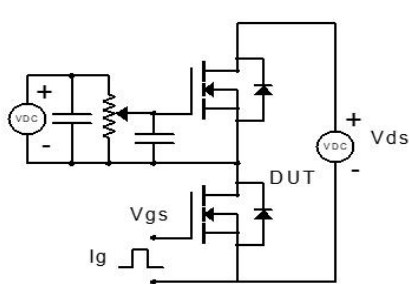


Figure 1: Gate Charge Test Circuit & Waveform

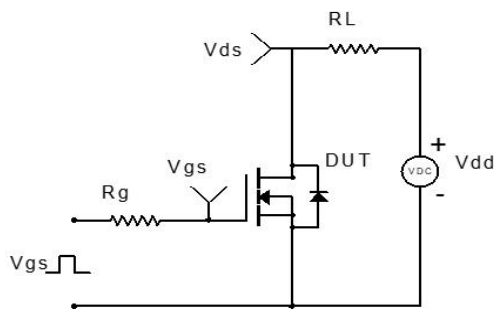


Figure 2: Resistive Switching Test Circuit & Waveform

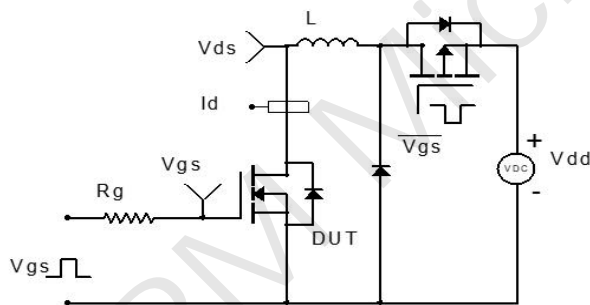


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

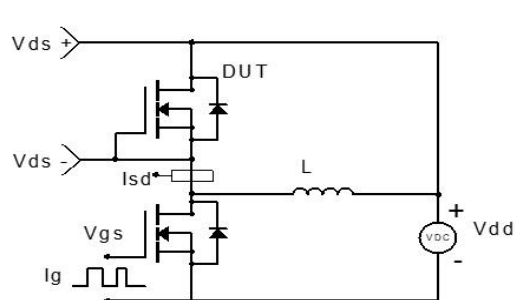
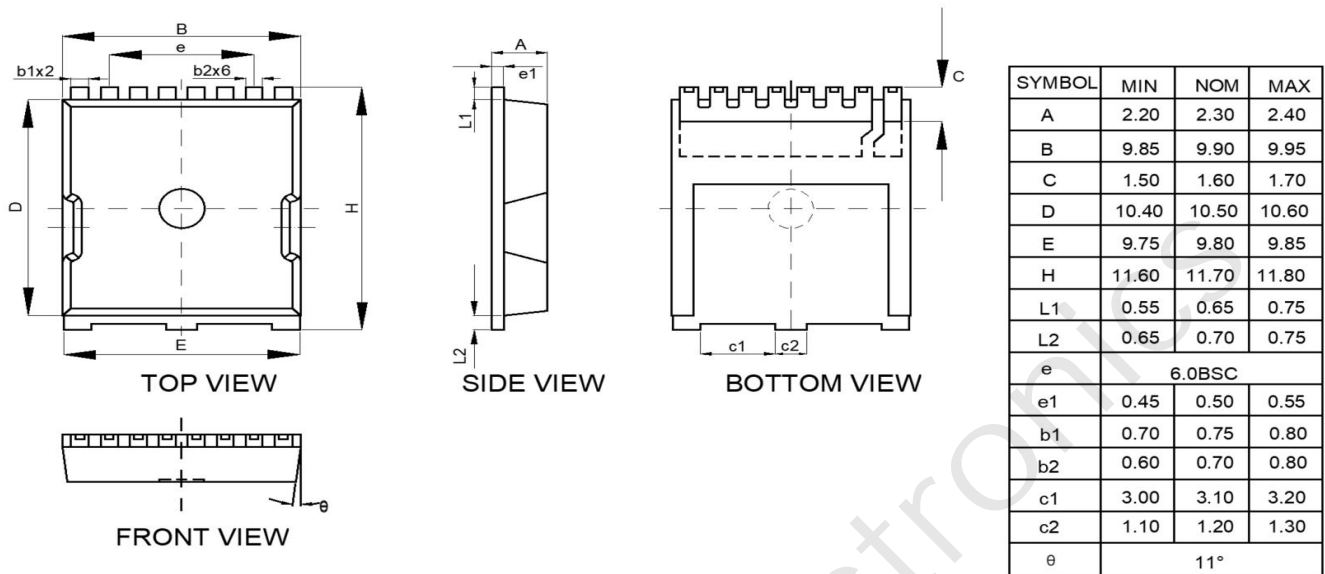


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TOLL)




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