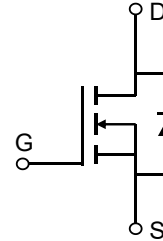


### Description

#### Features

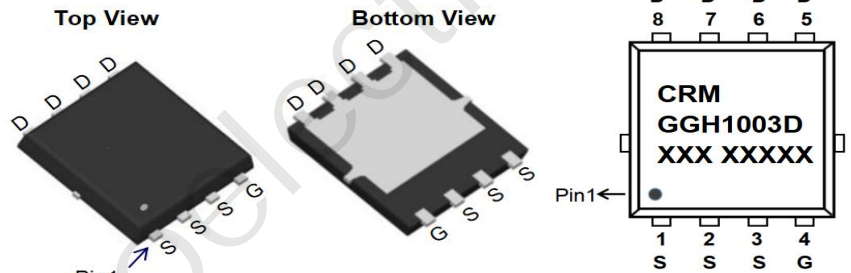
- 100V, 165A  
 $R_{DS(ON)}$  Typ = 2.5mΩ @  $V_{GS} = 10V$
- Advanced Split Gate Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- 100% UIS TESTED!
- 100%  $\Delta V_{ds}$  TESTED!



Schematic Diagram

#### Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

#### Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMGGH1003D	CRMGGH1003D	PDFN5x6-8L	TAPING	13"	5000	60000

#### Absolute Maximum Ratings (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V <sub>DS</sub>	Drain-to-Source Voltage	100	V	
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	165	A
		T <sub>C</sub> = 100°C	99	A
I <sub>DM</sub>	Pulsed Drain Current <sup>(1)</sup>	660	A	
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>(2)</sup>	473	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	171	W
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	0.73	°C/W	
T <sub>J</sub> , T <sub>STG</sub>	Junction & Storage Temperature Range	-55 to 150	°C	

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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#### Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

#### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.4	2.8	3.6	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	2.5	3.2	mΩ

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 50\text{V},$ $f = 1\text{MHz}$	-	3832	-	pF
$C_{oss}$	Output Capacitance		-	1546	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	20	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 50\text{V}, I_D = 20\text{A}$	-	68	-	nC
$Q_{gs}$	Gate Source Charge		-	16.5	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	15	-	nC

#### Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 50\text{V}$ $I_D = 40\text{A}, R_{GEN} = 3\Omega$	-	18.5	-	ns
$t_r$	Turn-On Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	18	-	ns
$t_f$	Turn-Off Fall Time		-	15.5	-	ns

#### Drain-Source Diode Characteristics and Max Ratings

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	165	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	660	A
$V_{SD}$	Drain to Source Diode Forward Voltage		-	-	1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time		-	78	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	170	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2.  $E_{AS}$  condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 50\text{V}$ ,  $V_G = 10\text{V}$ ,  $R_G = 25\Omega$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 43.5\text{A}$
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

## Typical Performance Characteristics

Figure 1: Output Characteristics

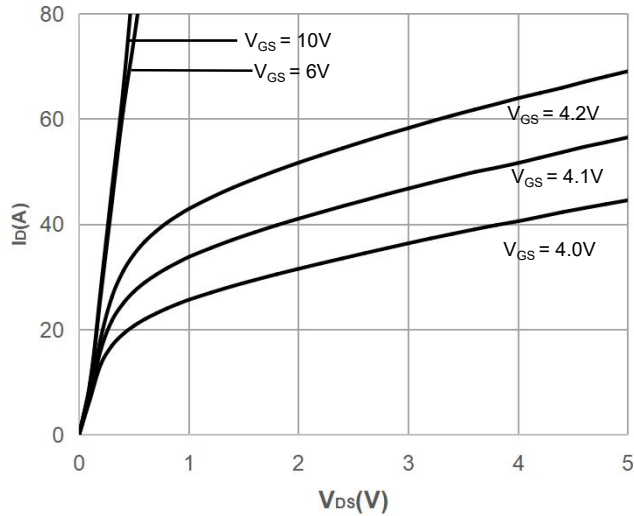


Figure 2: Typical Transfer Characteristics

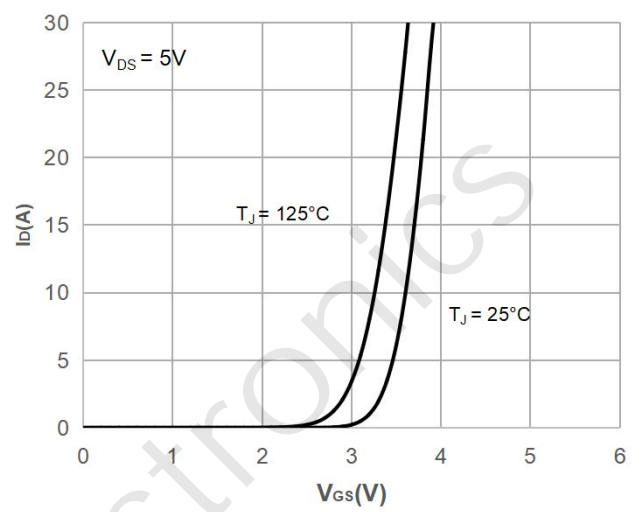


Figure 3: On-resistance vs. Drain Current

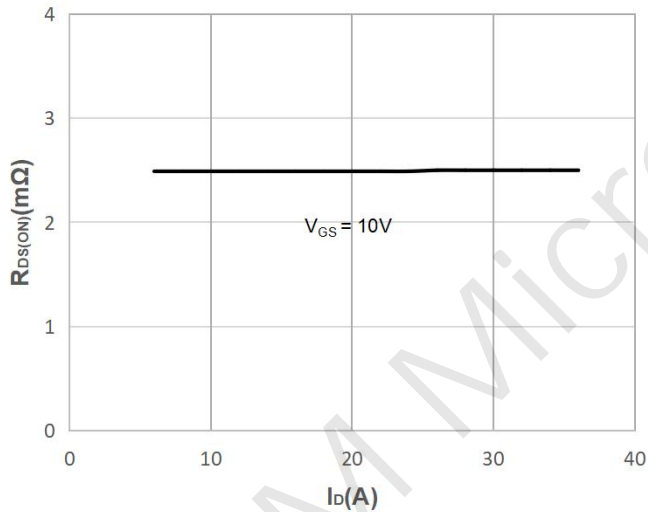


Figure 4: Body Diode Characteristics

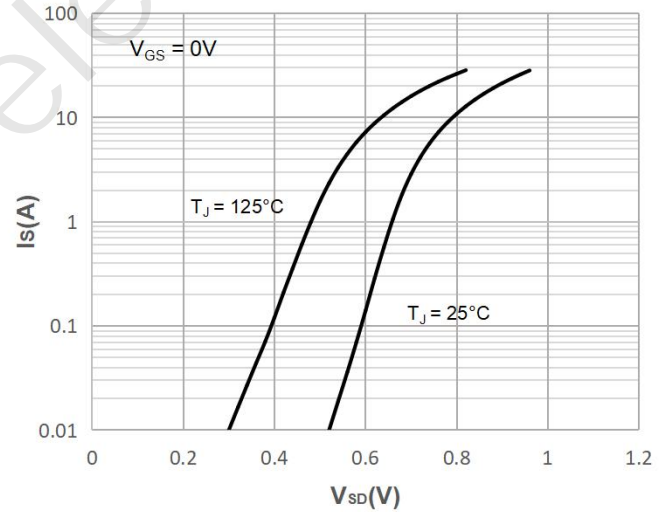


Figure 5: Gate Charge Characteristics

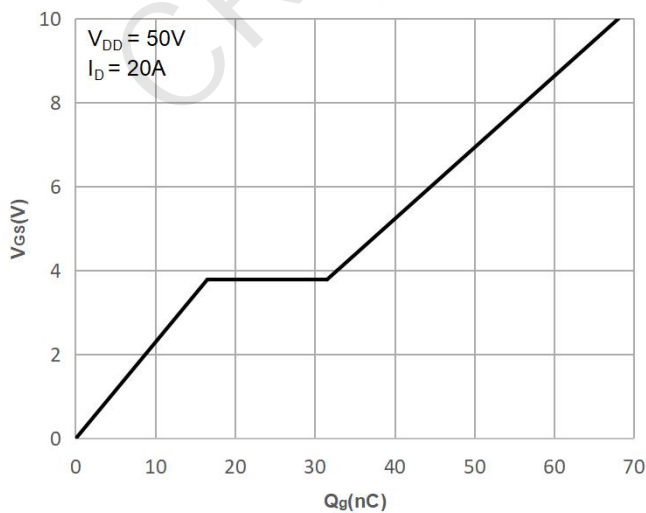
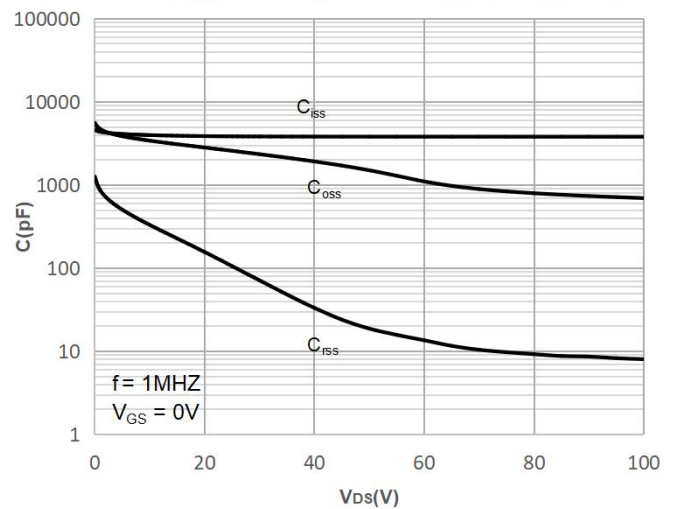


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

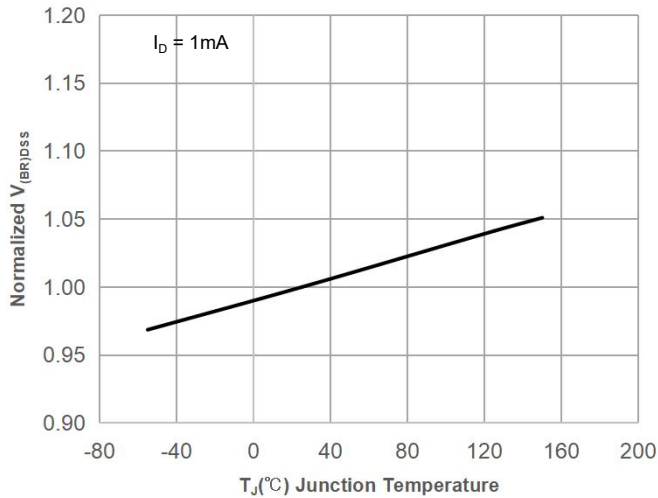


Figure 8: Normalized on Resistance vs. Junction Temperature

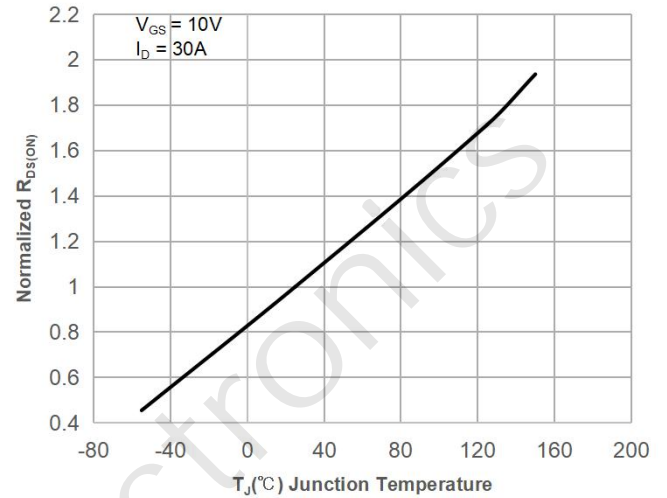


Figure 9: Maximum Safe Operating Area

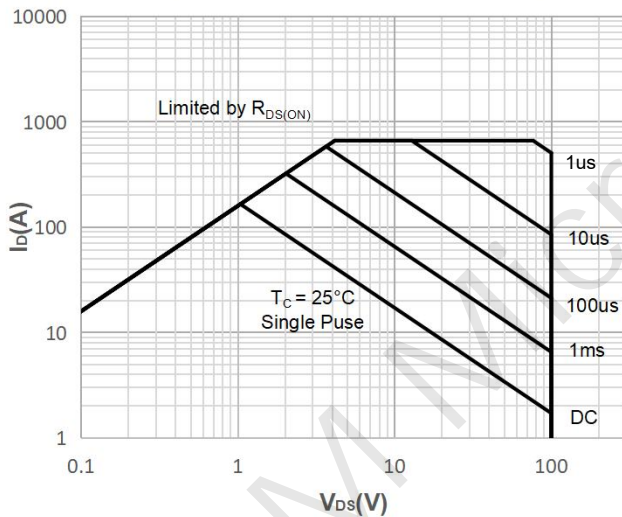


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

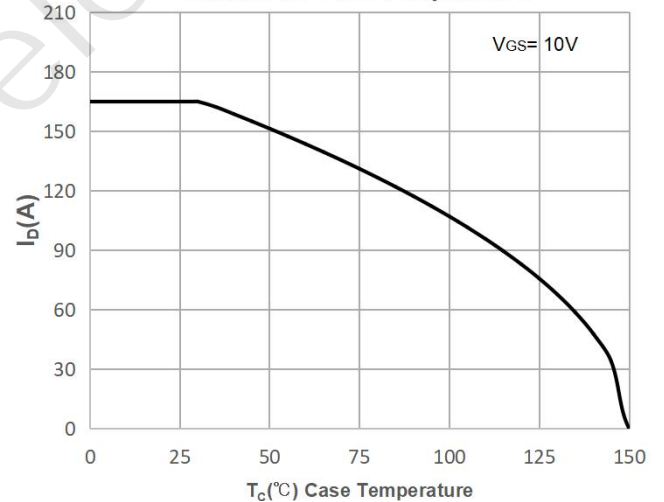


Figure 11: Normalized Maximum Transient Thermal Impedance

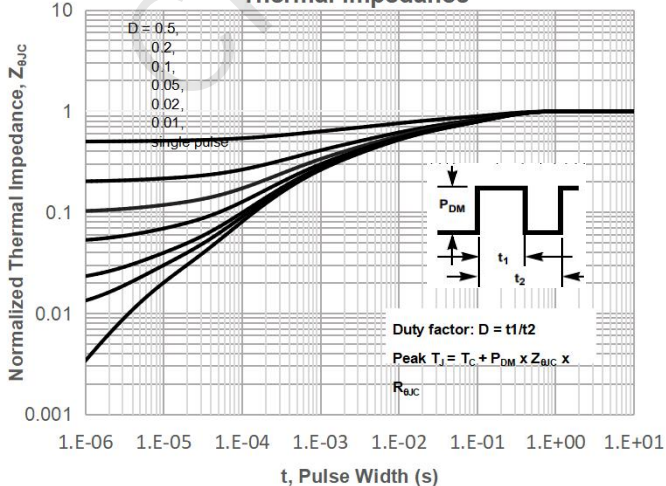
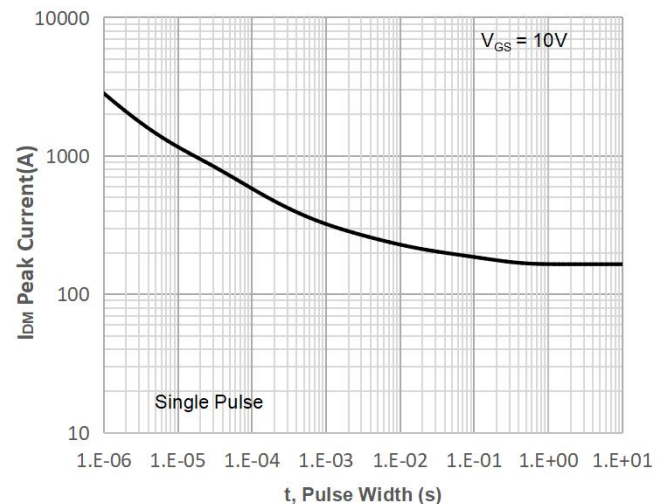


Figure 12: Peak Current Capacity



## Test Circuit

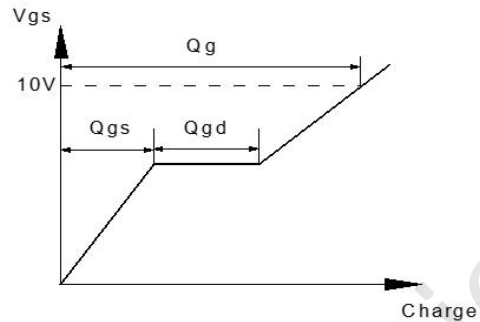
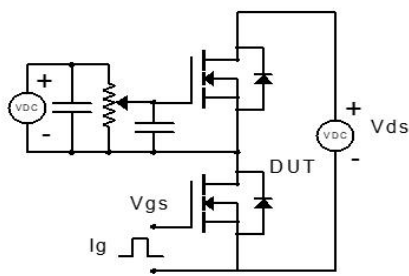


Figure 1: Gate Charge Test Circuit & Waveform

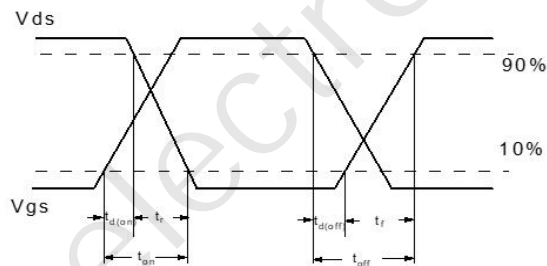
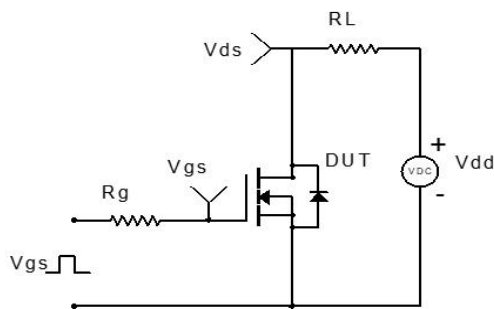


Figure 2: Resistive Switching Test Circuit & Waveform

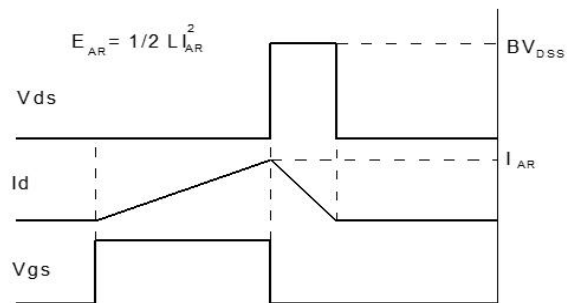
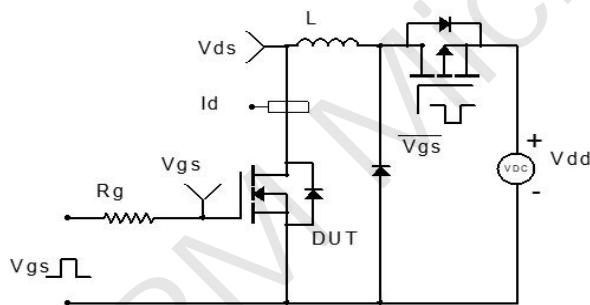


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

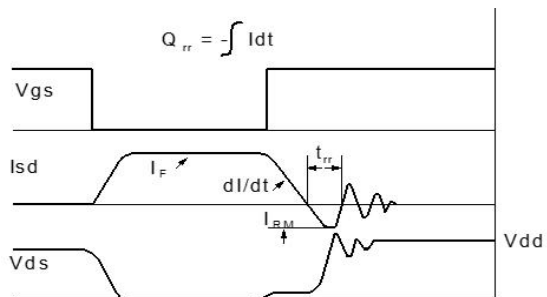
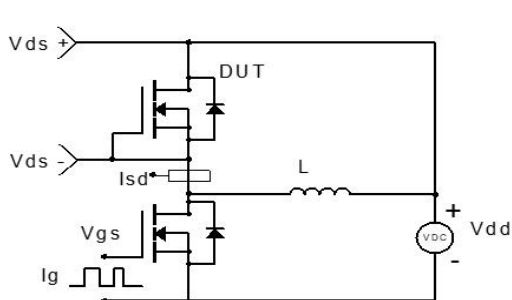
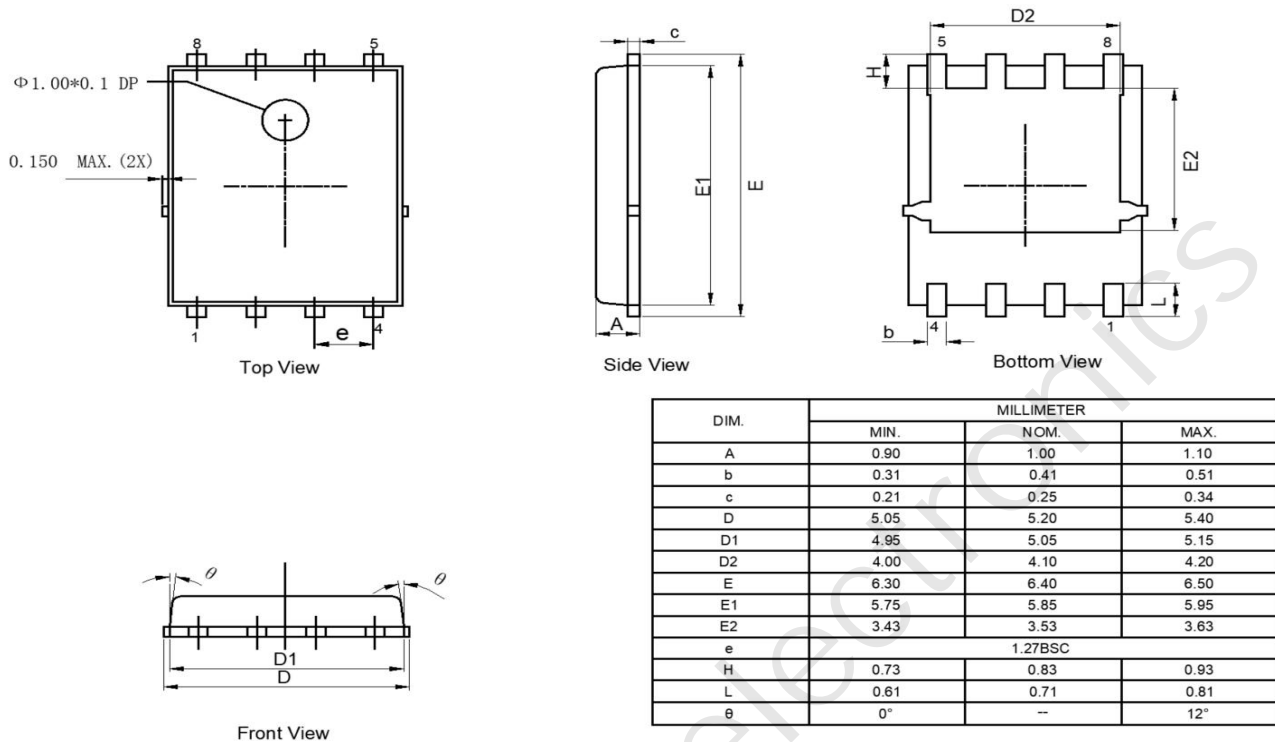


Figure 4: Diode Recovery Test Circuit & Waveform

### Package Mechanical Data(PDFN5x6-8L)




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