

### Description

#### Features

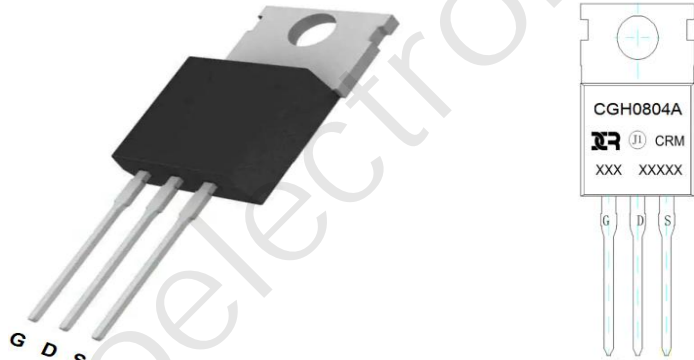
- 80V, 130A  
 $R_{DS(ON)}$  Typ = 3.9mΩ @  $V_{GS} = 10V$   
 Advanced Split Gate Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- 100% UIS TESTED!
- 100%  $\Delta V_{ds}$  TESTED!



Schematic Diagram

#### Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

#### Package Marking and Ordering Information

Device	Marking	Package	Outline	TUBE(pcs)	Inner Box (pcs)	Per Carton (pcs)
CRMCGH0804A	CRMCGH0804A	TO-220C-3L	TUBE	50	1000	5000

#### Absolute Maximum Ratings (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V <sub>DS</sub>	Drain-to-Source Voltage	80	V	
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	130	A
		T <sub>C</sub> = 100°C	78	A
I <sub>DM</sub>	Pulsed Drain Current <sup>(1)</sup>	520	A	
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>(2)</sup>	400	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	147	W
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	0.85	°C/W	
T <sub>J</sub> , T <sub>STG</sub>	Junction & Storage Temperature Range	-55 to 150	°C	

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
--------	-----------	------------	------	------	------	------

#### Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

#### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	3.9	5.1	mΩ

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V},$ $f = 1\text{MHz}$	-	4850	-	pF
$C_{oss}$	Output Capacitance		-	787	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	16	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 40\text{V}, I_D = 20\text{A}$	-	68	-	nC
$Q_{gs}$	Gate Source Charge		-	23	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	15	-	nC

#### Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 40\text{V}$ $I_D = 20\text{A}, R_{GEN} = 3\Omega$	-	20	-	ns
$t_r$	Turn-On Rise Time		-	38	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	30	-	ns
$t_f$	Turn-Off Fall Time		-	15	-	ns

#### Drain-Source Diode Characteristics and Max Ratings

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	130	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	520	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 20A, di/dt = 100A/us	-	48	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	100	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2.  $E_{AS}$  condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 40\text{V}$ ,  $V_G = 10\text{V}$ ,  $R_G = 25\text{ohm}$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 40\text{A}$
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

## Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveform

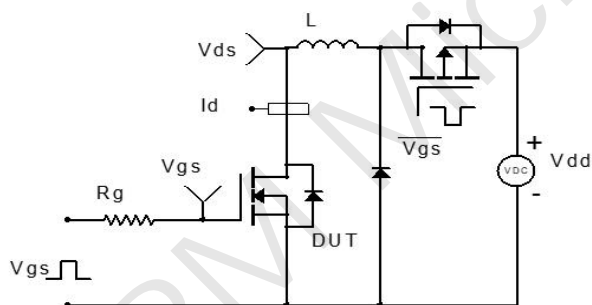


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

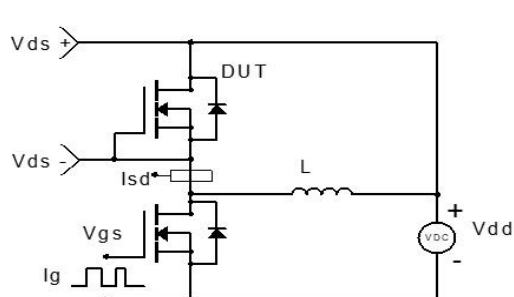
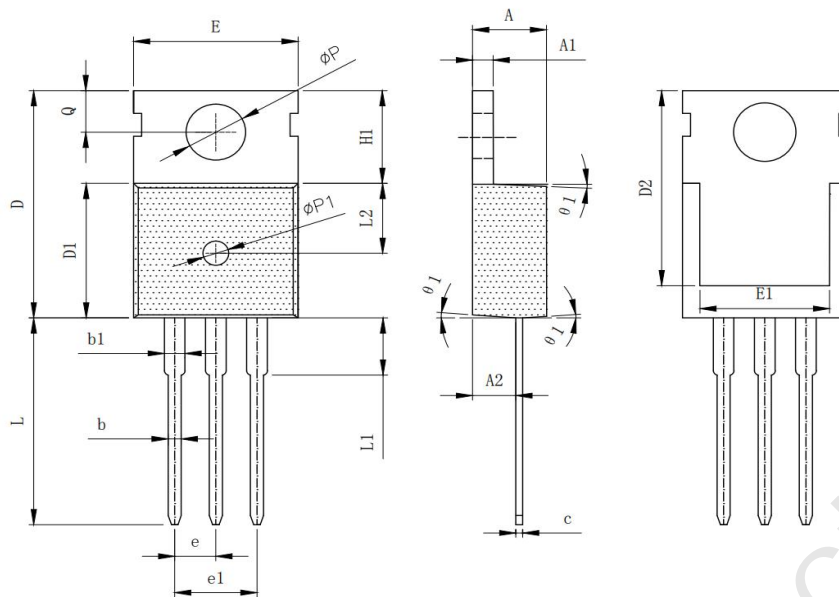


Figure 4: Diode Recovery Test Circuit & Waveform

### Package Mechanical Data(TO-220C-3L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.25	1.30	1.35
A2	2.30	2.40	2.50
b	0.70	0.80	0.90
b1	1.25	1.35	1.45
c	0.40	0.50	0.60
D	15.50	15.80	16.10
D1	9.10	9.20	9.30
D2	12.73	12.83	12.93
E	9.70	9.90	10.20
E1	7.60	8.00	8.40
e	2.54 (BSC)		
e1	5.08 (BSC)		
H1	6.30	6.50	6.80
L	12.75	13.08	13.50
L1	—	—	3.10
L2	4.30	4.60	4.90
ϕP	3.50	3.60	3.70
ϕP1	1.40	1.50	1.60
Q	2.70	—	2.90
θ 1	2°	4°	6°


NOTES: 1. PKG SURFACE IS MATTE Ra1.2~1.4;  
 OTHERS IS POLISHED Ra0.15;

### Important Notice

The information presented in datasheets is for reference only. CRM reserves the right to make changes at any time to any products or information herein, without notice.

Customers are responsible for the design and applications, including compliance with all laws, regulations and safety requirements or standards.

“Typical” parameters which provided in datasheets can vary in different applications and actual performance may vary over time. Customers are responsible for doing all necessary testing to minimize the risks associated with their applications and products.

 is a registered trademark of Wuxi CRM Microelectronics Co. , Ltd.

Copyright ©2023 CRM Microelectronics Co. , Ltd. All rights reserved.

### Contact information

For more information, please visit: <http://www.crm-semi.tech>

For sales information, please send an email to: [sales@crm-semi.com](mailto:sales@crm-semi.com)