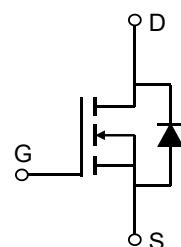


### Description

### Features

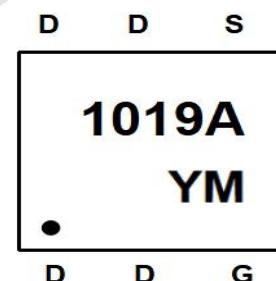
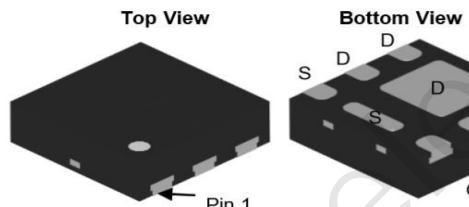
- 100V, 14A
- $R_{DS(ON)}$  Typ = 20.5mΩ @  $V_{GS}$  = 10V
- $R_{DS(ON)}$  Typ = 25.3mΩ @  $V_{GS}$  = 4.5V
- Advanced Split Gate Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free



Schematic Diagram

### Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

### Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMVGL1019A	1019A	DFN2020-6L	TAPING	7"	3000	120000

### Absolute Maximum Ratings (@ $T_J$ = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current $T_C = 25^\circ\text{C}$	14	A
	$T_C = 100^\circ\text{C}$	8.4	A
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	56	A
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	8.9	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	14	°C/W
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	°C

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

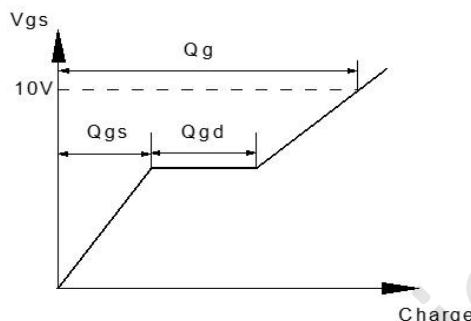
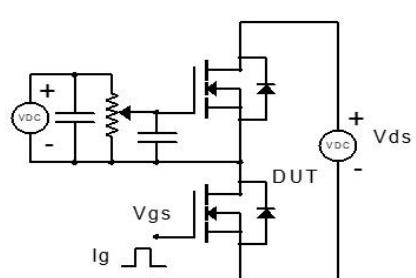
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.2	1.8	2.4	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance <sup>(2)</sup>	$V_{GS} = 10\text{V}, I_D = 5\text{A}$	-	20.5	26.7	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 3\text{A}$	-	25.3	32.9	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance		-	660	-	pF
$C_{\text{oss}}$	Output Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	375	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	21	-	pF
$Q_g$	Total Gate Charge		-	25	-	nC
$Q_{gs}$	Gate Source Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 50\text{V}, I_D = 10\text{A}$	-	6	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	5	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On DelayTime		-	14	-	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10\text{V}, V_{DD} = 50\text{V}$	-	12	-	ns
$t_{d(off)}$	Turn-Off DelayTime	$I_D = 10\text{A}, R_{\text{GEN}} = 3\Omega$	-	23	-	ns
$t_f$	Turn-Off Fall Time		-	6	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	14	A
$I_{\text{SM}}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	56	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
$trr$	Body Diode Reverse Recovery Time		-	50	-	ns
$Qrr$	Body Diode Reverse Recovery Charge	$I_F = 10\text{A}, di/dt = 100\text{A/us}$	-	90	-	nC

Notes:

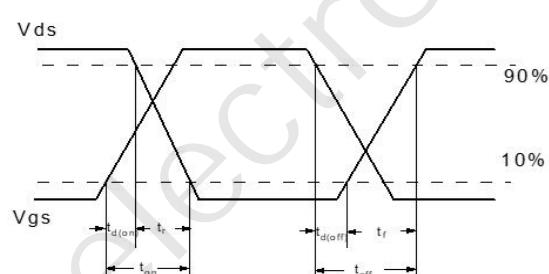
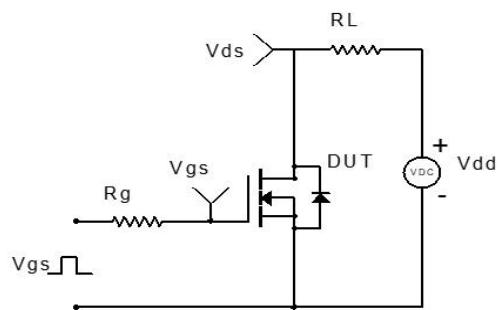
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

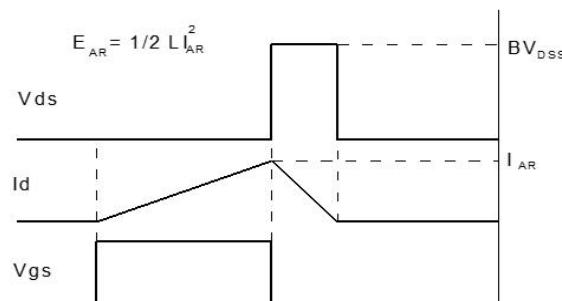
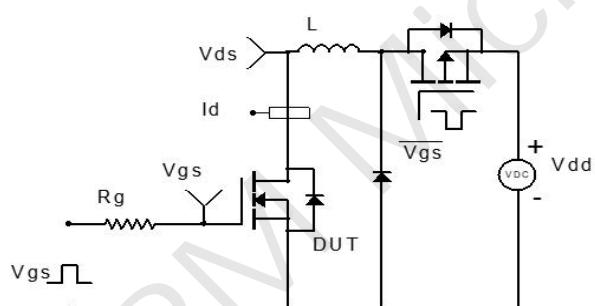
## Test Circuit



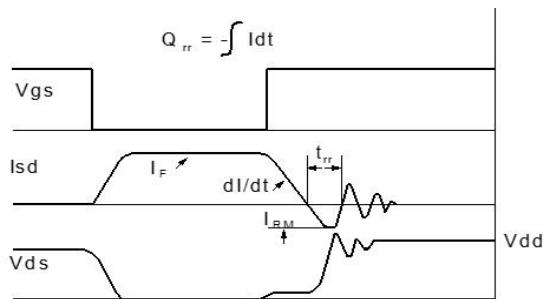
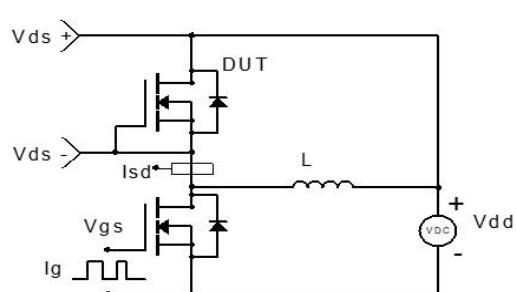
**Figure 1: Gate Charge Test Circuit & Waveform**



**Figure 2: Resistive Switching Test Circuit & Waveform**

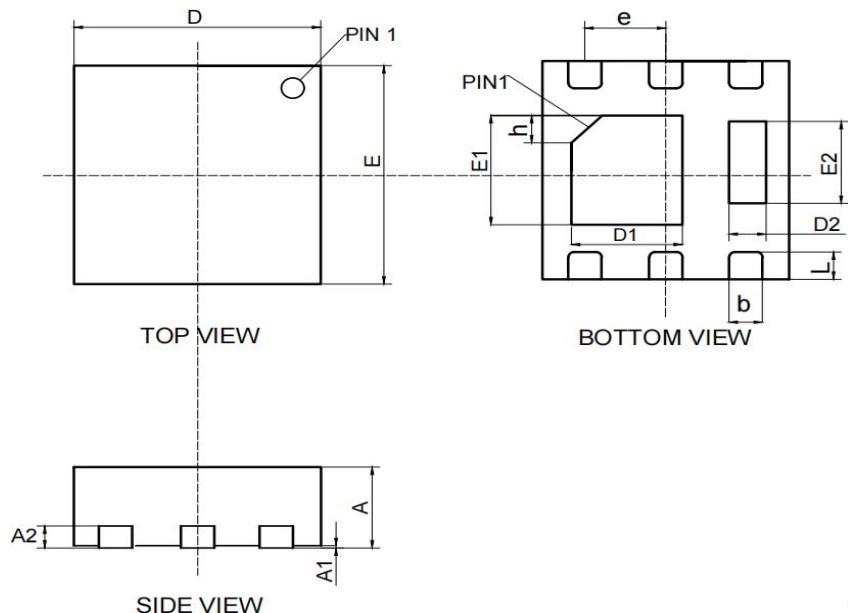


**Figure 3: Unclamped Inductive Switching Test Circuit& Waveform**



**Figure 4: Diode Recovery Test Circuit & Waveform**

## Package Mechanical Data(DFN2020-6L)



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	NA	0.02	0.05
A2	0.18	0.20	0.25
b	0.20	0.27	0.34
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
e	0.65 BSC		

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## Contact information

For more information, please visit: <http://www.crm-semi.tech>

For sales information, please send an email to: [sales@crm-semi.com](mailto:sales@crm-semi.com)