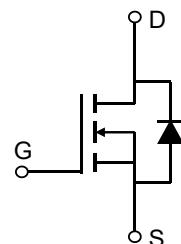


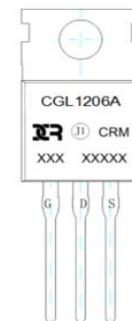
Description

Features

- 120V, 90A
- $R_{DS(ON)}$ Typ = 6.6mΩ @ V_{GS} = 10V
- $R_{DS(ON)}$ Typ = 7.6mΩ @ V_{GS} = 4.5V
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS TESTED!
- 100% ΔV_{ds} TESTED!



Schematic Diagram



Marking and Pin Assignment

Application

- Load Switch
- PWM Application
- Power Management

Package Marking and Ordering Information

Device	Marking	Package	Outline	TUBE(pcs)	Inner Box (pcs)	Per Carton (pcs)
CRMCG1206A	CRMCG1206A	TO-220C-3L	TUBE	50	1000	5000

Absolute Maximum Ratings (@ T_J = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	120	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	360	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	225	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.93	°C/W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	120	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.4	1.9	2.6	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	6.6	8.6	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	-	7.6	9.9	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance		-	3364	-	pF
C_{oss}	Output Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}, f = 1\text{MHz}$	-	624	-	pF
C_{rss}	Reverse Transfer Capacitance		-	9.6	-	pF
Q_g	Total Gate Charge		-	40	-	nC
Q_{gs}	Gate Source Charge	$V_{GS} = 0 \text{ to } 10\text{V}$	-	9	-	nC
Q_{gd}	Gate Drain("Miller") Charge	$V_{DS} = 60\text{V}, I_D = 20\text{A}$	-	10	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime		-	13	-	ns
t_r	Turn-On Rise Time	$V_{GS} = 10\text{V}, V_{DD} = 60\text{V}$	-	25	-	ns
$t_{d(off)}$	Turn-Off DelayTime	$I_D = 30\text{A}, R_{\text{GEN}} = 6\Omega$	-	38	-	ns
t_f	Turn-Off Fall Time		-	34	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	90	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	360	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time		-	65	-	ns
Qrr	Body Diode Reverse Recovery Charge	$I_F = 15\text{A}, di/dt = 100\text{A/us}$	-	70	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=0.5\text{mH}$, $I_{AS}=30\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

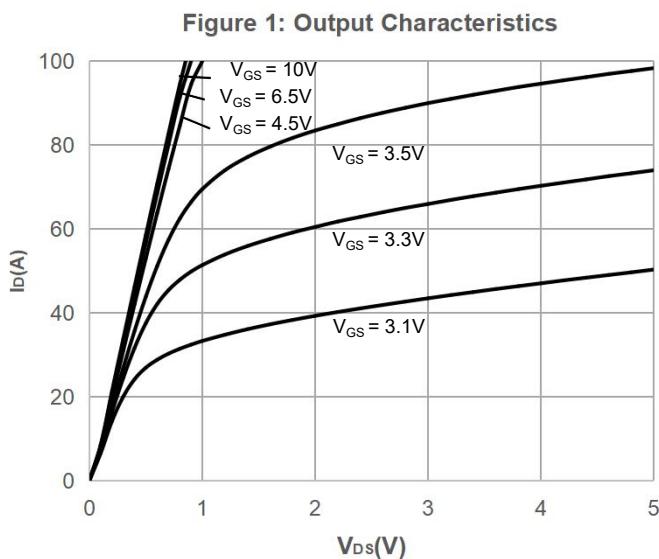


Figure 2: Typical Transfer Characteristics

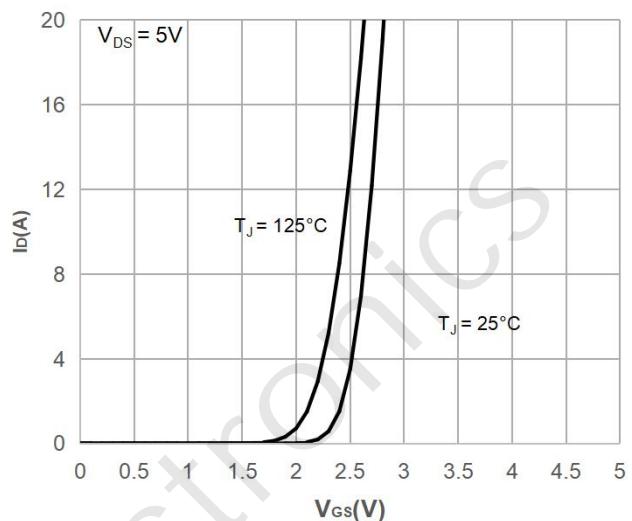


Figure 3: On-resistance vs. Drain Current

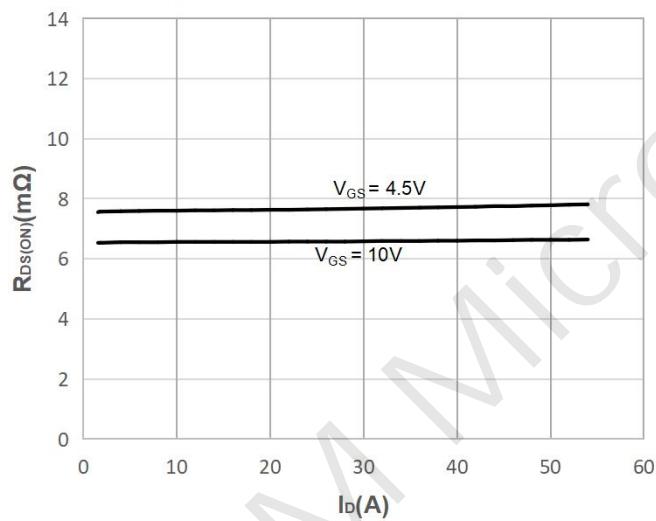


Figure 4: Body Diode Characteristics

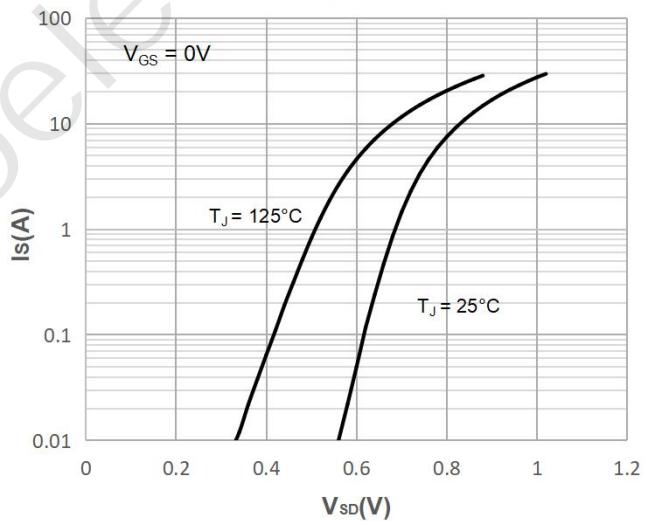


Figure 5: Gate Charge Characteristics

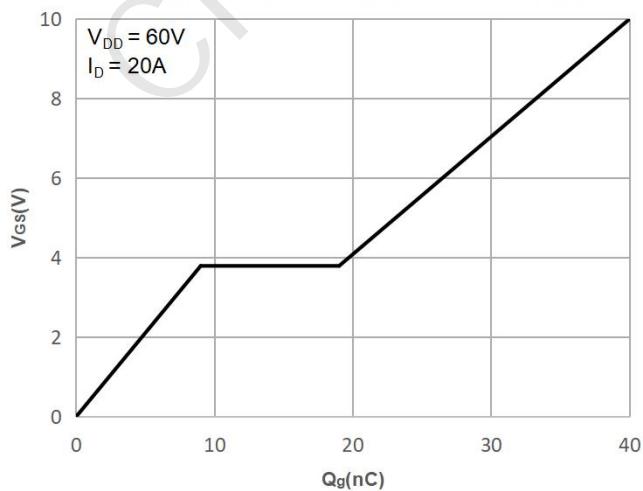
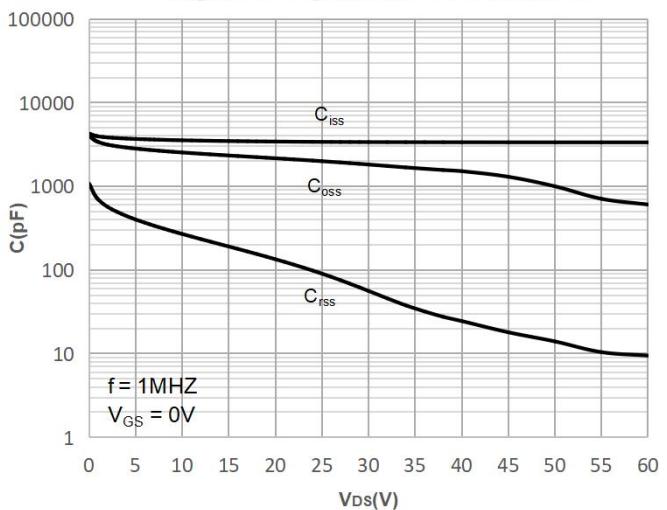


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

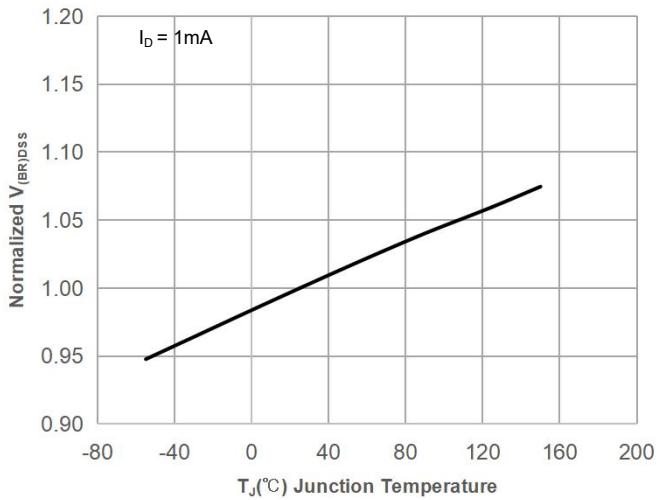


Figure 8: Normalized on Resistance vs. Junction Temperature

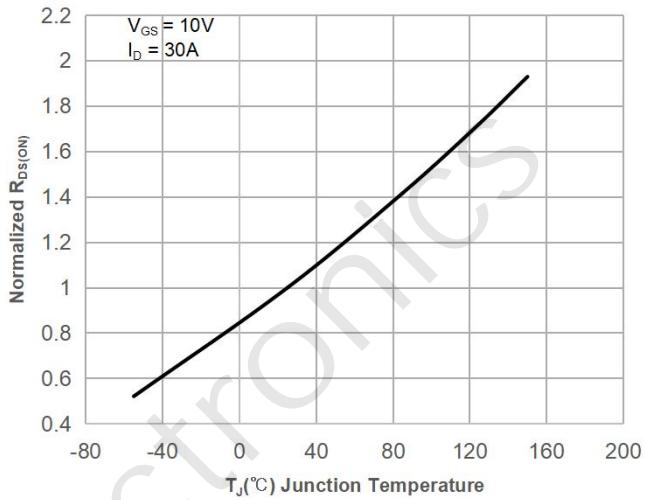


Figure 9: Maximum Safe Operating Area

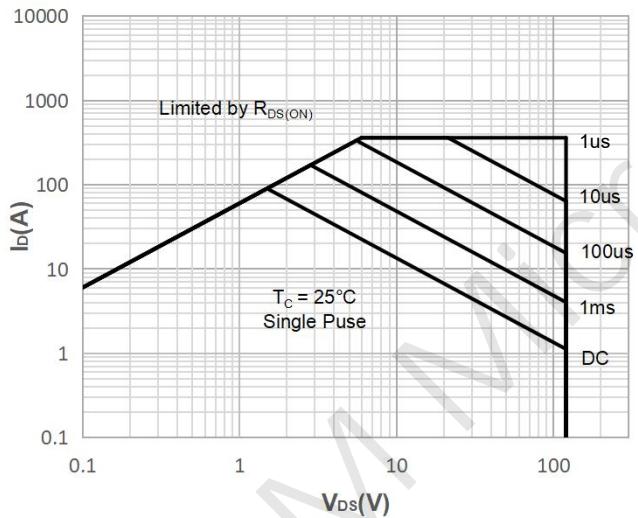


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

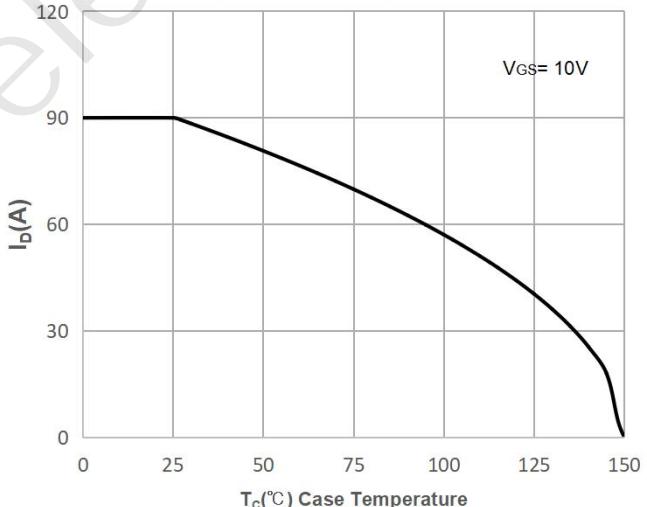


Figure 11: Normalized Maximum Transient Thermal Impedance

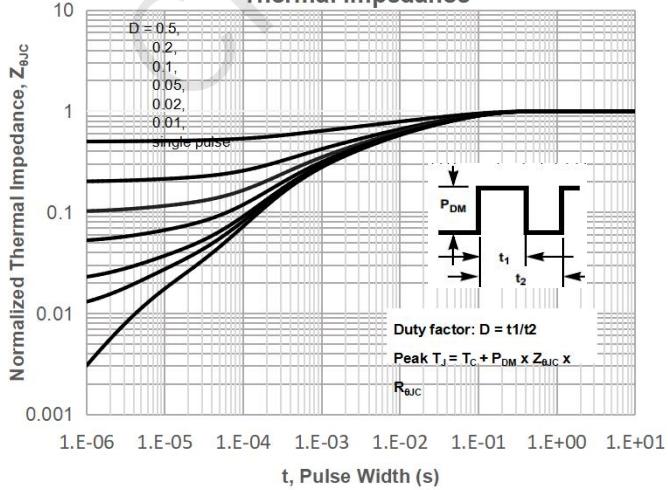
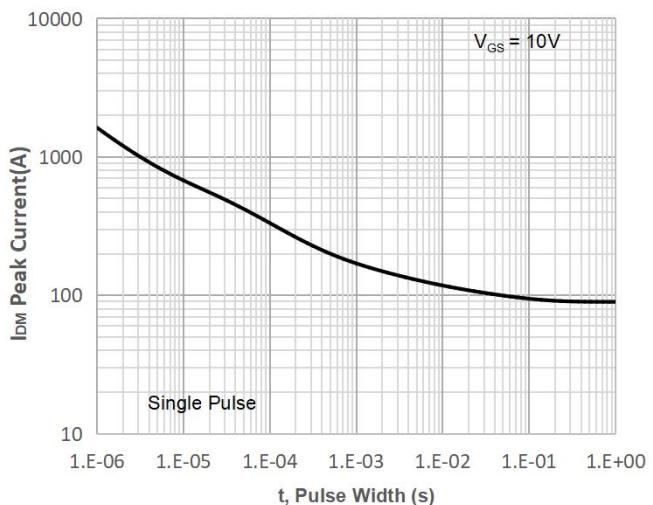


Figure 12: Peak Current Capacity



Test Circuit

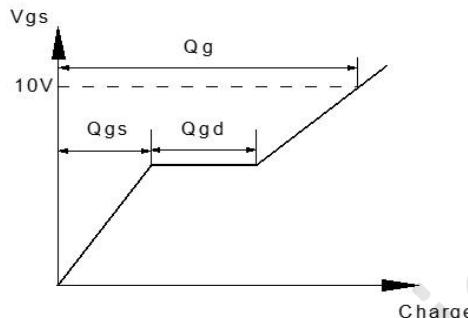
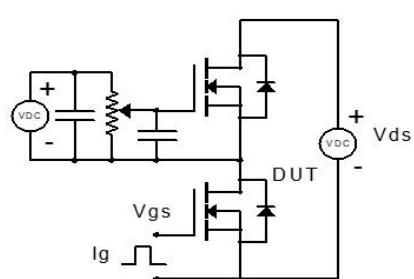


Figure 1: Gate Charge Test Circuit & Waveform

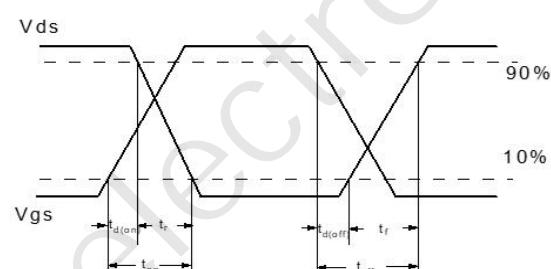
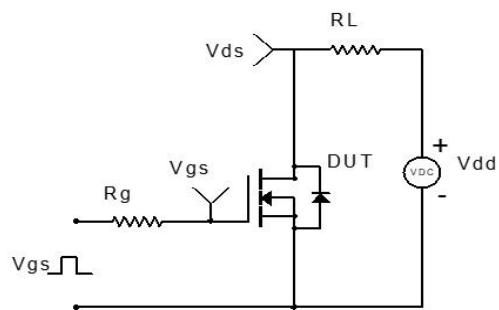


Figure 2: Resistive Switching Test Circuit & Waveform

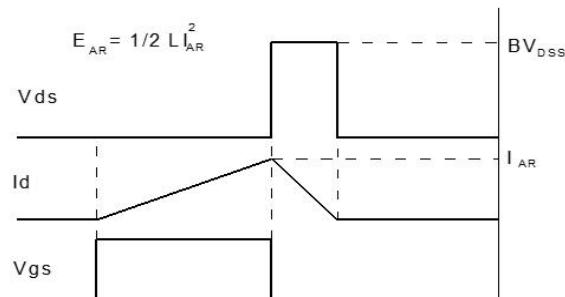
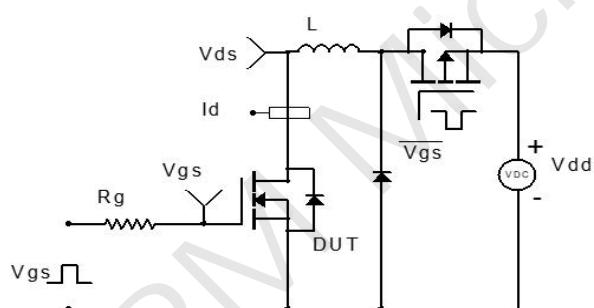


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

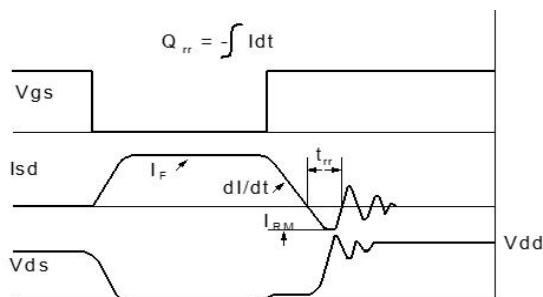
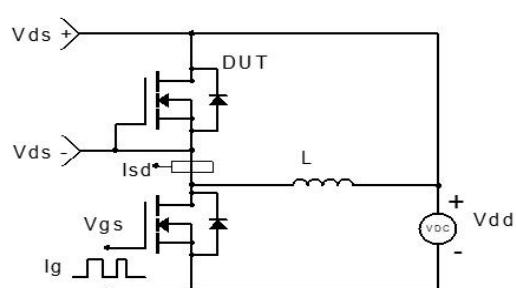
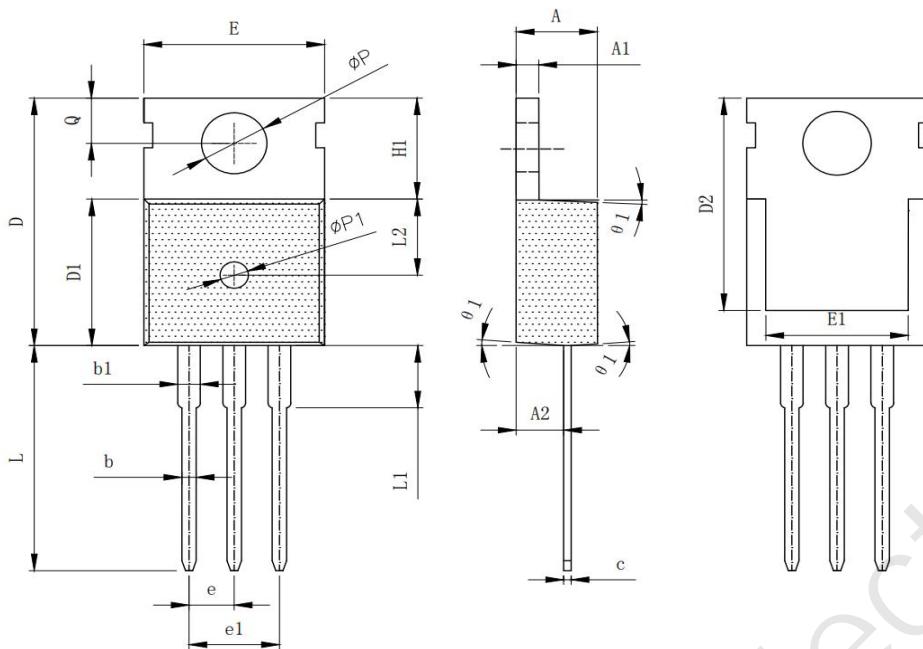


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-220C-3L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.25	1.30	1.35
A2	2.30	2.40	2.50
b	0.70	0.80	0.90
b1	1.25	1.35	1.45
c	0.40	0.50	0.60
D	15.50	15.80	16.10
D1	9.10	9.20	9.30
D2	12.73	12.83	12.93
E	9.70	9.90	10.20
E1	7.60	8.00	8.40
e	2.54	(BSC)	
e1	5.08	(BSC)	
H1	6.30	6.50	6.80
L	12.75	13.08	13.50
L1	—	—	3.10
L2	4.30	4.60	4.90
φP	3.50	3.60	3.70
φP1	1.40	1.50	1.60
Q	2.70	—	2.90
θ1	2°	4°	6°

NOTES: 1. PKG ■ SURFACE IS MATTE Ra1.2~1.4;
OTHERS IS POLISHED Ra0.15;

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