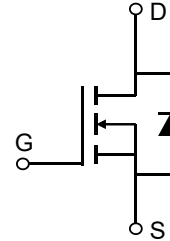


Description

Features

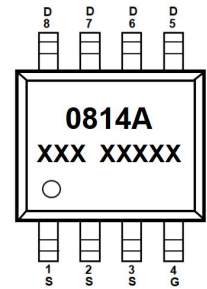
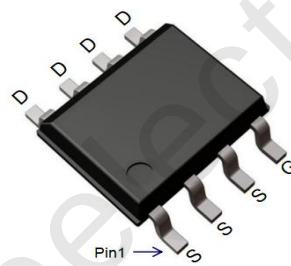
- 85V, 9A
- $R_{DS(ON)}$ Typ = 14mΩ @ $V_{GS} = 10V$
- $R_{DS(ON)}$ Typ = 17.5mΩ @ $V_{GS} = 4.5V$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free
- 100% UIS TESTED!



Schematic Diagram

Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMPGL0814A	0814A	SOP-8	TAPING	13"	4000	40000

Absolute Maximum Ratings (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	85	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	9
		$T_A = 100^\circ\text{C}$	5.4
I_{DM}	Pulsed Drain Current ⁽¹⁾	36	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	36	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.5
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	50	°C/W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	85	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 85\text{V}$, $V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1	1.6	2	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}$, $I_D = 5\text{A}$	-	14	18.2	mΩ
		$V_{GS} = 4.5\text{V}$, $I_D = 3\text{A}$	-	17.5	22.8	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 40\text{V}$, $f = 1\text{MHz}$	-	729	-	pF
C_{oss}	Output Capacitance		-	205	-	pF
C_{rss}	Reverse Transfer Capacitance		-	6	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0$ to 10V $V_{DS} = 40\text{V}$, $I_D = 10\text{A}$	-	32	-	nC
Q_{gs}	Gate Source Charge		-	7	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	6	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}$, $V_{DD} = 40\text{V}$ $I_D = 10\text{A}$, $R_{GEN} = 3\Omega$	-	10	-	ns
t_r	Turn-On Rise Time		-	7	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	16	-	ns
t_f	Turn-Off Fall Time		-	8	-	ns

Drain-Source Diode Characteristics and Max Ratings

I_S	Maximum Continuous Drain to Source Diode Forward Current	$V_{GS} = 0\text{V}$, $I_S = 10\text{A}$	-	-	9	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	36	A
V_{SD}	Drain to Source Diode Forward Voltage		-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time		-	35	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	55	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 40\text{V}$, $V_G = 10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$, $I_{AS} = 12\text{A}$
3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Test Circuit

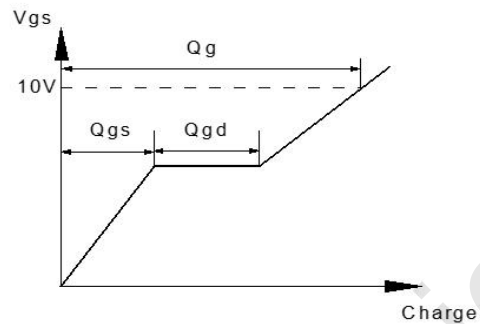
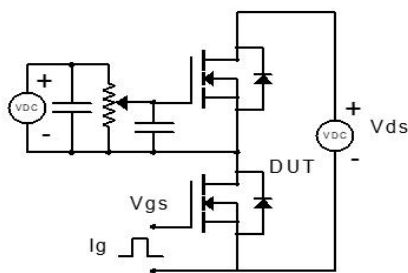


Figure 1: Gate Charge Test Circuit & Waveform

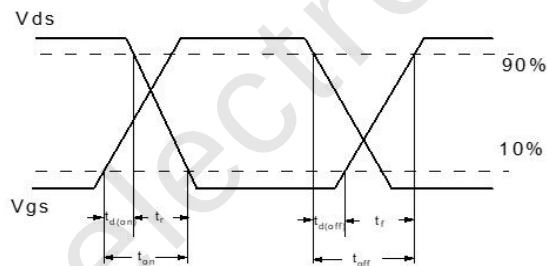
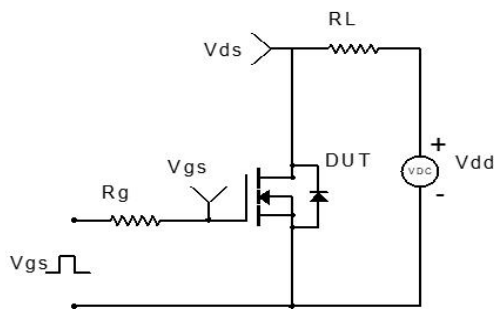


Figure 2: Resistive Switching Test Circuit & Waveform

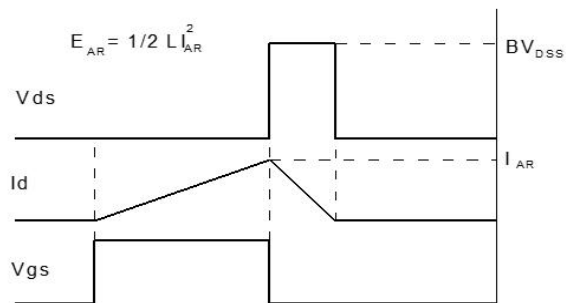
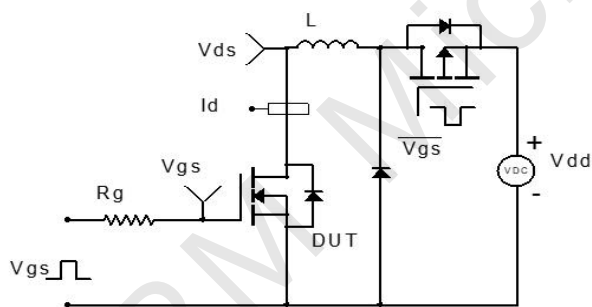


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

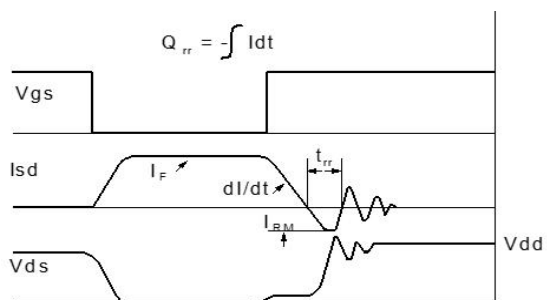
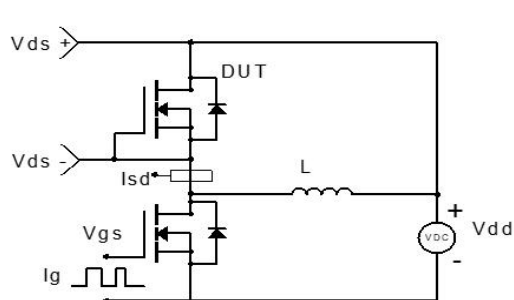
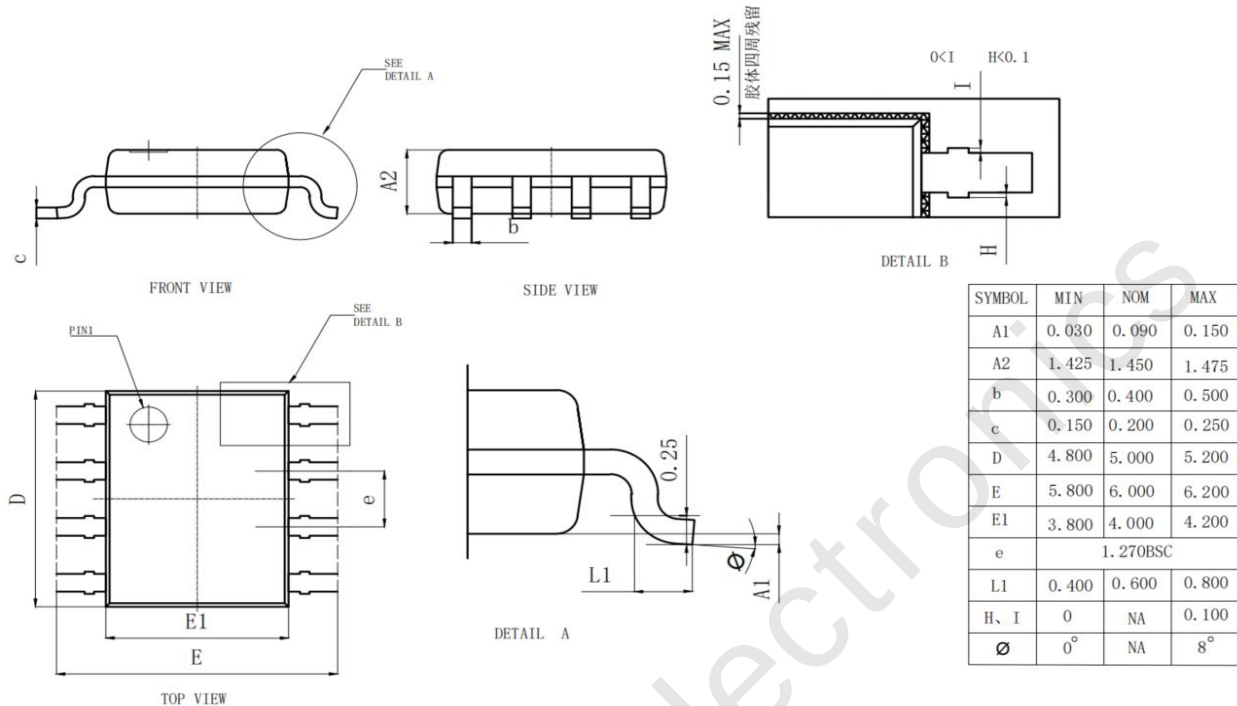


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOP-8)



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