

### Description

#### Features

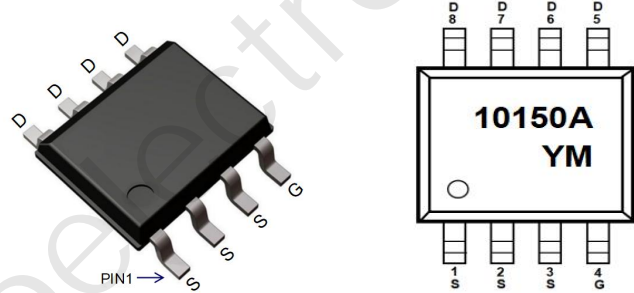
- 100V, 3A  
 $R_{DS(ON)}$  Typ = 118mΩ @  $V_{GS} = 10V$   
 $R_{DS(ON)}$  Typ = 126mΩ @  $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free
- 100% UIS TESTED!



Schematic Diagram

#### Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

#### Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMPTL10150A	10150A	SOP-8	TAPING	13"	4000	40000

#### Absolute Maximum Ratings (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ\text{C}$	3
		$T_A = 100^\circ\text{C}$	1.8
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	12	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>	12	mJ
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$	3
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(3)</sup>	42	°C/W
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	°C

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
--------	-----------	------------	------	------	------	------

#### Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$ , $V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

#### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1.2	1.7	2.2	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(4)</sup>	$V_{GS} = 10\text{V}$ , $I_D = 2\text{A}$	-	118	153	mΩ
		$V_{GS} = 4.5\text{V}$ , $I_D = 1\text{A}$	-	126	164	mΩ

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	655	-	pF
$C_{oss}$	Output Capacitance		-	31	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	24	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0$ to $10\text{V}$ $V_{DS} = 50\text{V}$ , $I_D = 3\text{A}$	-	14.8	-	nC
$Q_{gs}$	Gate Source Charge		-	3	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	4.4	-	nC

#### Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}$ , $V_{DD} = 50\text{V}$ $I_D = 3\text{A}$ , $R_{GEN} = 3\Omega$	-	12	-	ns
$t_r$	Turn-On Rise Time		-	7.6	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	36	-	ns
$t_f$	Turn-Off Fall Time		-	9.2	-	ns

#### Drain-Source Diode Characteristics and Max Ratings

$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = 3\text{A}$	-	-	1.2	V

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
  2.  $E_{AS}$  condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 50\text{V}$ ,  $V_G = 10\text{V}$ ,  $R_G = 25\Omega$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 7\text{A}$
  3.  $R_{\theta JA}$  is measured with the device mounted on a  $1\text{inch}^2$  pad of 2oz copper FR4 PCB
  4. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

## Typical Performance Characteristics

Figure 1: Output Characteristics

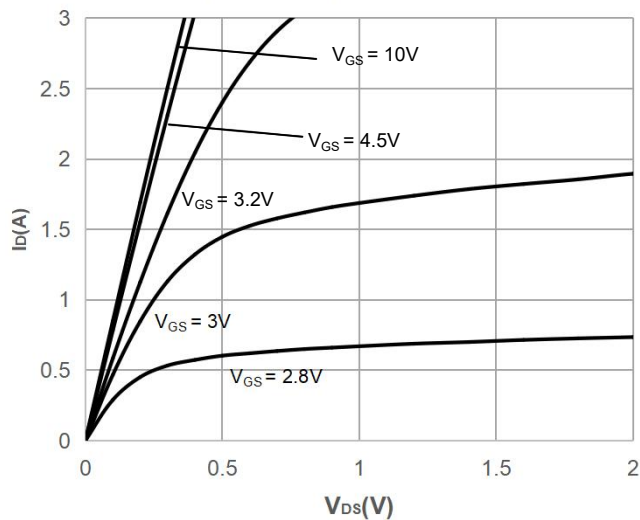


Figure 2: Typical Transfer Characteristics

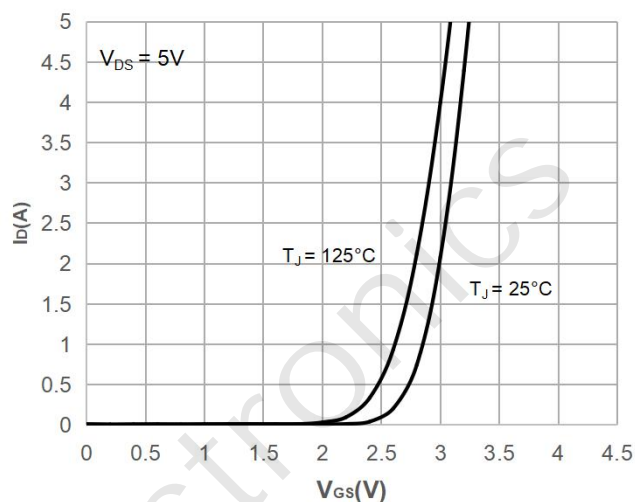


Figure 3: On-resistance vs. Drain Current

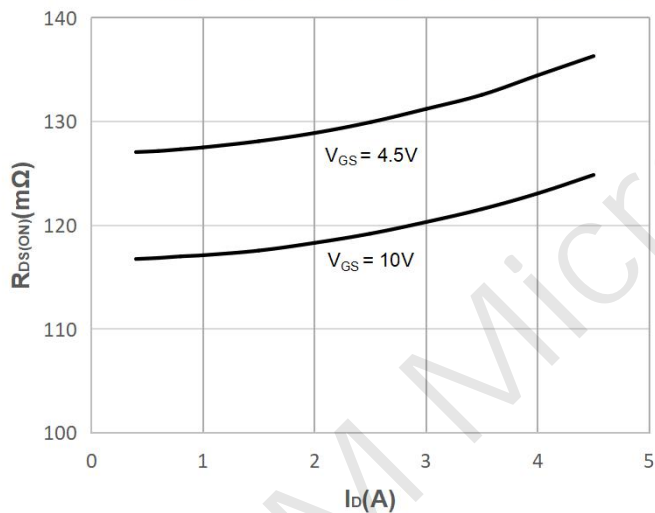


Figure 4: Body Diode Characteristics

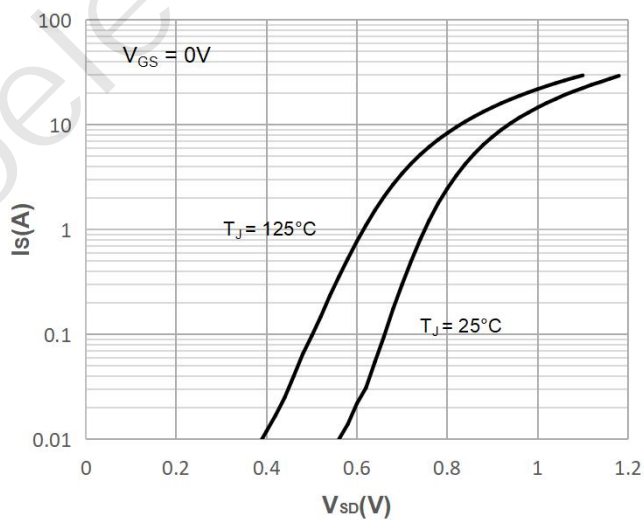


Figure 5: Gate Charge Characteristics

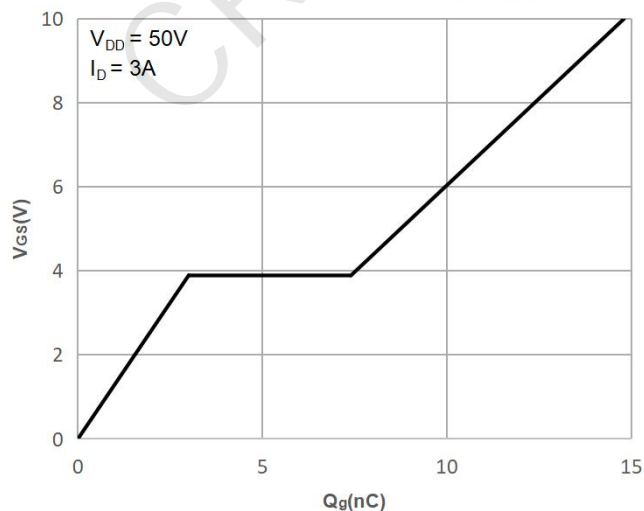
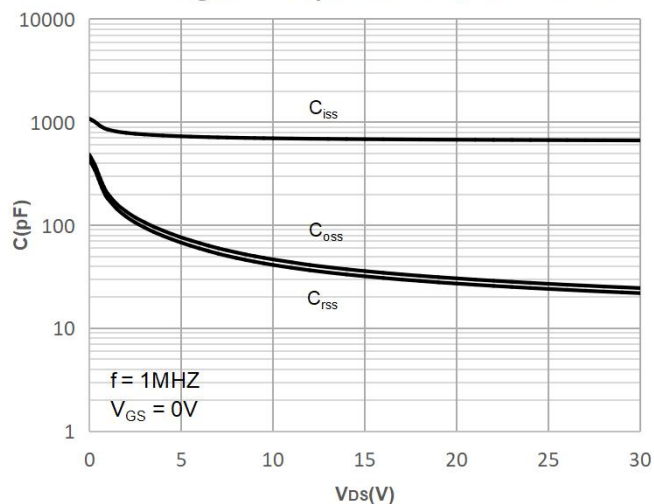


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

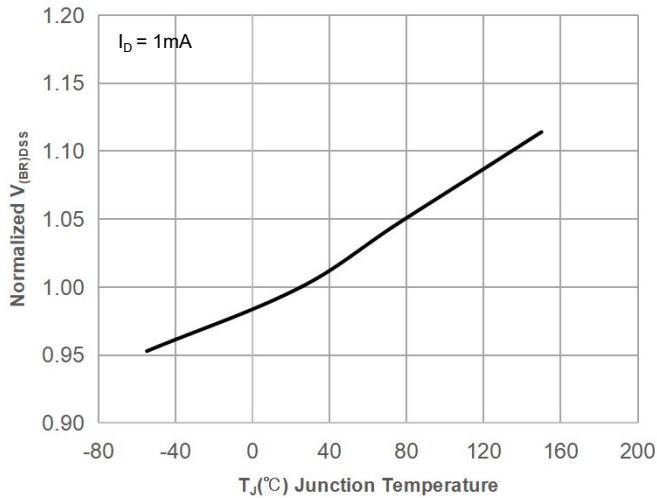


Figure 8: Normalized on Resistance vs. Junction Temperature

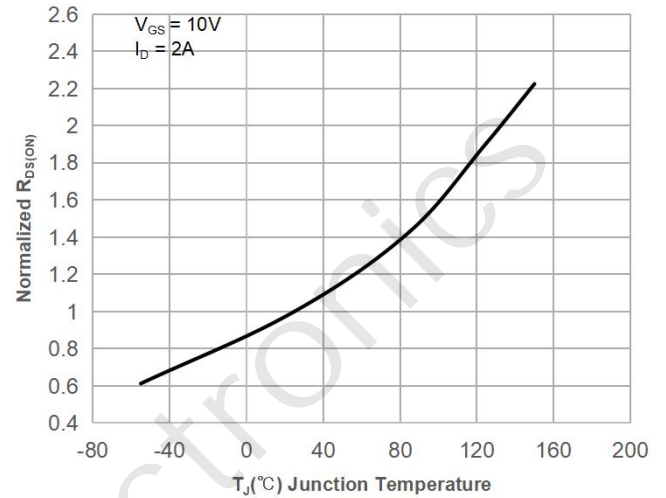


Figure 9: Maximum Safe Operating Area

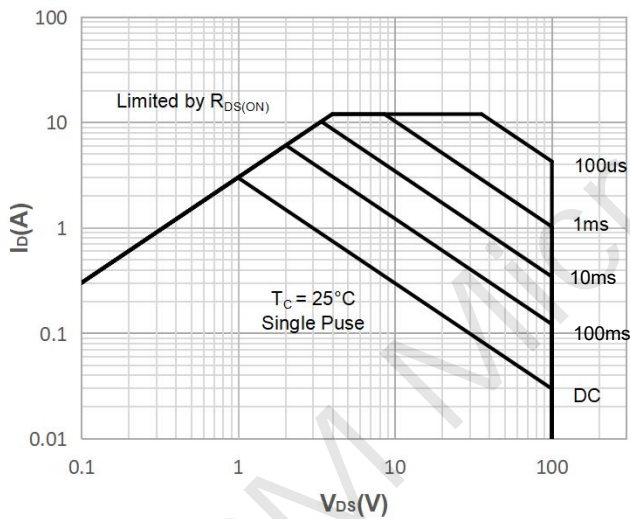


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

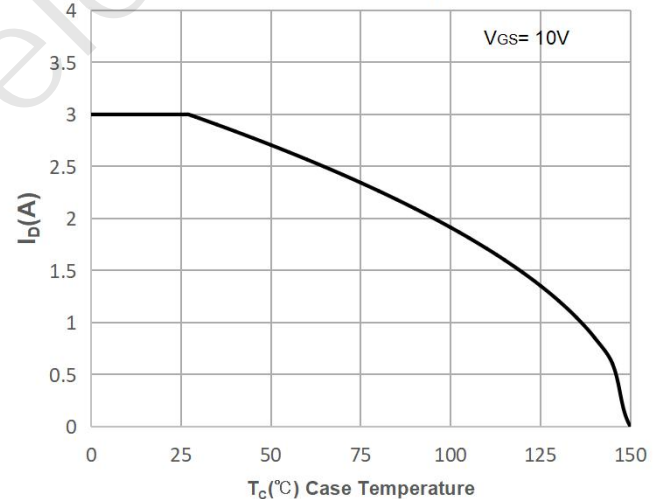


Figure 11: Normalized Maximum Transient Thermal Impedance

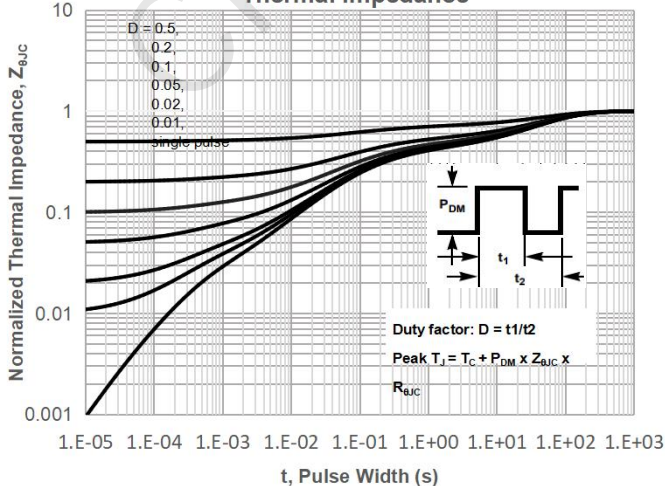
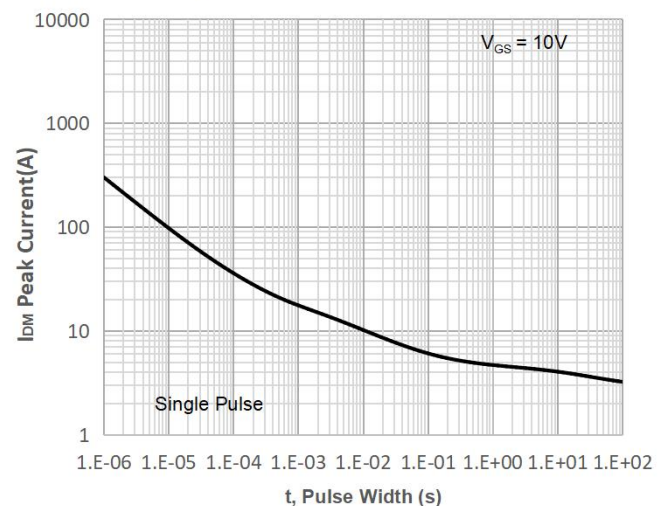


Figure 12: Peak Current Capacity



## Test Circuit

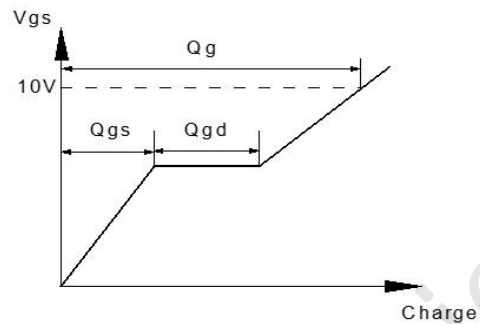


Figure 1: Gate Charge Test Circuit & Waveform

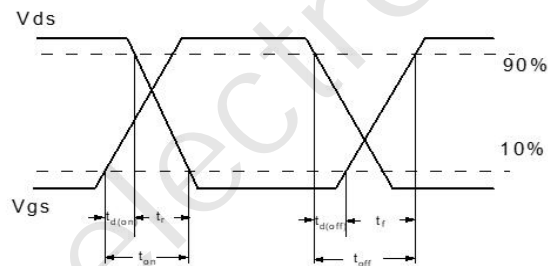
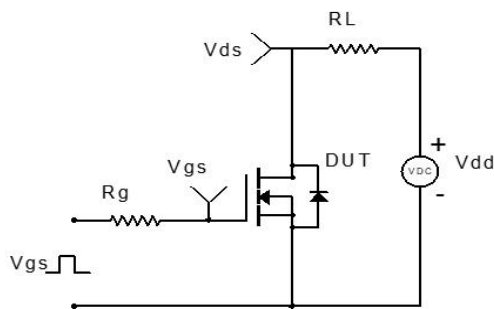


Figure 2: Resistive Switching Test Circuit & Waveform

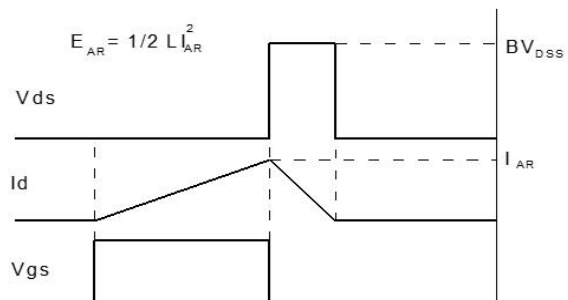
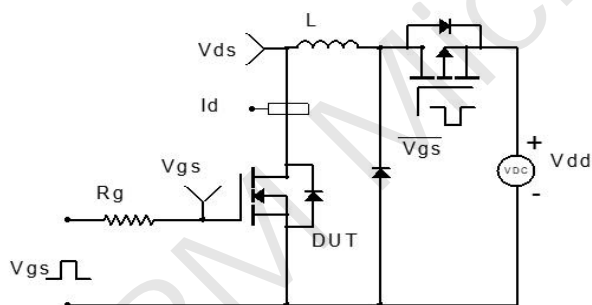


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

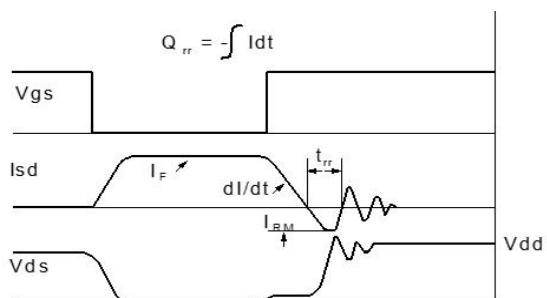
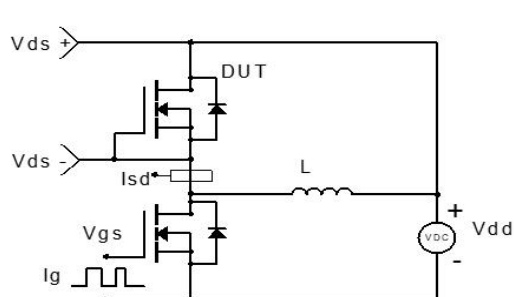
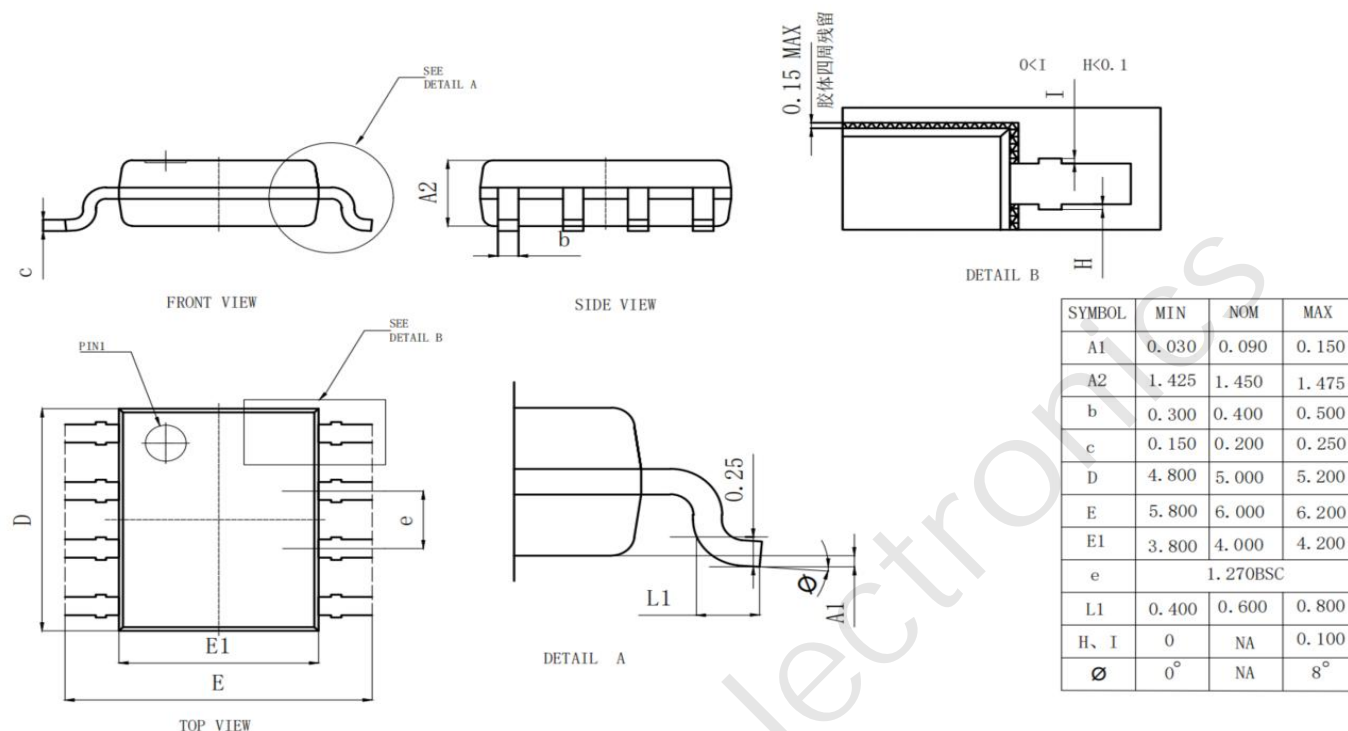


Figure 4: Diode Recovery Test Circuit & Waveform

### Package Mechanical Data(SOP-8)




### Important Notice

The information presented in datasheets is for reference only. CRM reserves the right to make changes at any time to any products or information herein, without notice.

Customers are responsible for the design and applications, including compliance with all laws, regulations and safety requirements or standards.

“Typical” parameters which provided in datasheets can vary in different applications and actual performance may vary over time. Customers are responsible for doing all necessary testing to minimize the risks associated with their applications and products.

 is a registered trademark of Wuxi CRM Microelectronics Co., Ltd.  
 Copyright ©2023 CRM Microelectronics Co., Ltd. All rights reserved.

### Contact information

For more information, please visit: <http://www.crm-semi.tech>

For sales information, please send an email to: [sales@crm-semi.com](mailto:sales@crm-semi.com)