

Description

Features

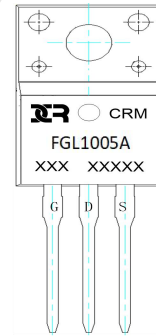
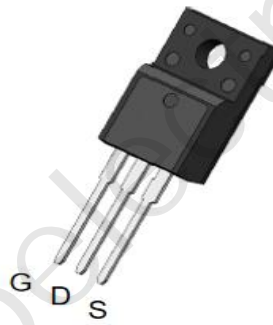
- 100V, 62A
- $R_{DS(ON)}$ Typ = 4.5mΩ @ $V_{GS} = 10V$
- $R_{DS(ON)}$ Typ = 5.7mΩ @ $V_{GS} = 4.5V$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS TESTED!
- 100% ΔV_{ds} TESTED!



Schematic Diagram

Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

Package Marking and Ordering Information

Device	Marking	Package	Outline	TUBE (pcs)	Inner Box (pcs)	Per Carton (pcs)
CRMFGL1005A	CRMFGL1005A	TO-220F-3L	TUBE	50	1000	5000

Absolute Maximum Ratings (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	62
		$T_C = 100^\circ\text{C}$	37.2
I_{DM}	Pulsed Drain Current ⁽¹⁾	248	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	248	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	39
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.2	°C/W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1.4	1.8	2.6	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}$, $I_D = 30\text{A}$	-	4.5	5.9	mΩ
		$V_{GS} = 4.5\text{V}$, $I_D = 25\text{A}$	-	5.7	7.4	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	-	4072	-	pF
C_{oss}	Output Capacitance		-	2140	-	pF
C_{rss}	Reverse Transfer Capacitance		-	56	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0$ to 10V $V_{DS} = 50\text{V}$, $I_D = 20\text{A}$	-	55	-	nC
Q_{gs}	Gate Source Charge		-	20	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	12	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}$, $V_{DD} = 30\text{V}$ $I_D = 30\text{A}$, $R_{GEN} = 3\Omega$	-	16	-	ns
t_r	Turn-On Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	30	-	ns
t_f	Turn-Off Fall Time		-	17	-	ns

Drain-Source Diode Characteristics and Max Ratings

I_S	Maximum Continuous Drain to Source Diode Forward Current	$V_{GS} = 0\text{V}$, $I_S = 30\text{A}$	-	-	62	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	248	A
V_{SD}	Drain to Source Diode Forward Voltage		-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time		-	60	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	120	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 0.5\text{mH}$, $I_{AS} = 31.5\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveform

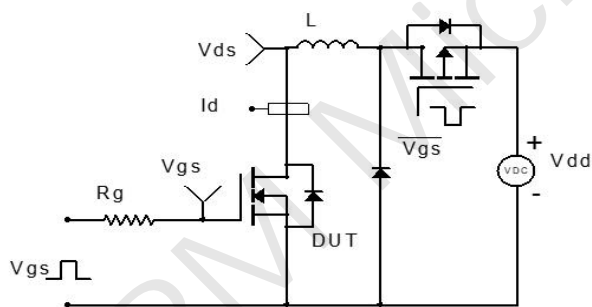
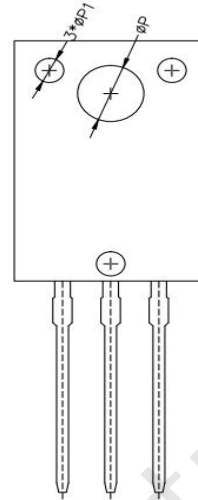
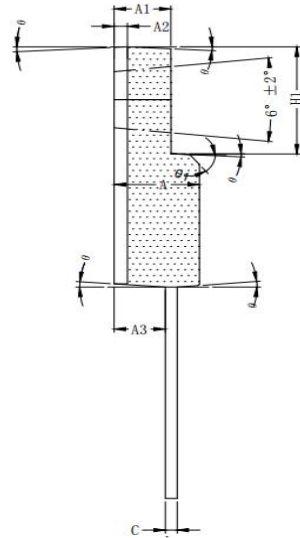
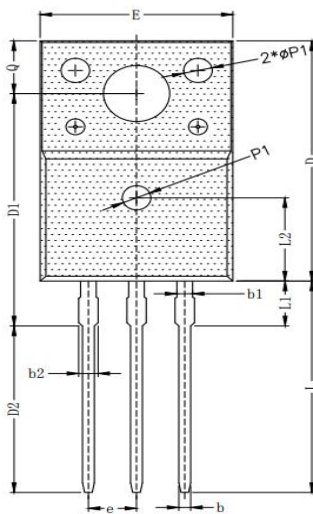


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform



Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-220F-3L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.50	4.70	4.83
A1	2.34	2.54	2.74
A2	0.70REF		
A3	2.56	2.76	2.93
b	0.70	---	0.90
b1	1.18	---	1.38
b2	---	---	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	9.60	9.80	10.00
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	3.10	3.20	3.30
L2	6.50REF		
φP	3.08	3.18	3.28
φP1	1.40	1.50	1.60
Q	3.20	---	3.40
θ	1°	5°	7°
θ 1	42°	45°	48°

NOTES:1. PKG SURFACE IS MATTE Ra1.2~1.4;
OTHERS IS POLISHED Ra0.15;

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