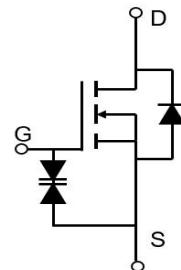


### Description

### Features

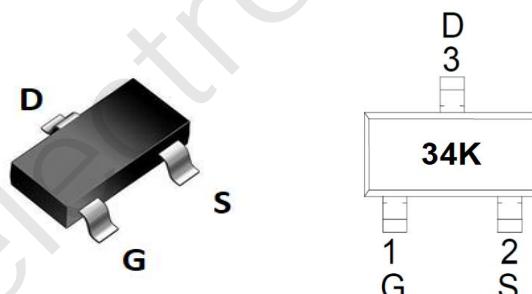
- 20V, 0.9A
- $R_{DS(ON)}$  Typ = 124mΩ @  $V_{GS}$  = 4.5V
- $R_{DS(ON)}$  Typ = 188mΩ @  $V_{GS}$  = 2.5V
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free
- ESD Protected: 2KV



Schematic Diagram

### Application

- Load Switch
- PWM Application
- Power Management



Marking and Pin Assignment

### Package Marking and Ordering Information

Device	Marking	Package	Outline	Reel Size	Reel (pcs)	Per Carton (pcs)
CRMLCTU3134K	34K	SOT-523-3L	TAPING	7"	3000	120000

### Absolute Maximum Ratings (@ $T_J$ = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$I_D$	Continuous Drain Current	0.9	A
		0.54	A
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	3.6	A
$P_D$	Power Dissipation	0.23	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(2)</sup>	540	°C/W
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	°C

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 10\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.4	0.65	1.0	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 4.5\text{V}, I_D = 0.5\text{A}$	-	124	162	$\text{m}\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 0.3\text{A}$	-	188	245	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance		-	60	-	pF
$C_{\text{oss}}$	Output Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 10\text{V}, f = 1\text{MHz}$	-	22	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	12	-	pF
$Q_g$	Total Gate Charge		-	1	-	nC
$Q_{gs}$	Gate Source Charge	$V_{GS} = 0$ to $4.5\text{V}$	-	0.28	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge	$V_{DS} = 10\text{V}, I_D = 0.9\text{A}$	-	0.22	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On DelayTime		-	2	-	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 4.5\text{V}, V_{DD} = 10\text{V}$	-	19	-	ns
$t_{d(off)}$	Turn-Off DelayTime	$I_D = 0.5\text{A}, R_{\text{GEN}} = 10\Omega$	-	10	-	ns
$t_f$	Turn-Off Fall Time		-	23	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.9	A
$I_{\text{SM}}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	3.6	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 0.9\text{A}$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2.  $R_{\theta\text{JA}}$  is measured with the device mounted on a 1inch<sup>2</sup> pad of 2oz copper FR4 PCB

3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

## Test Circuit

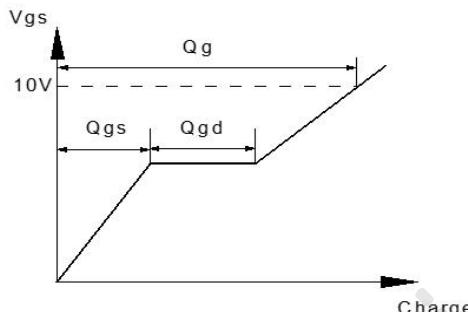
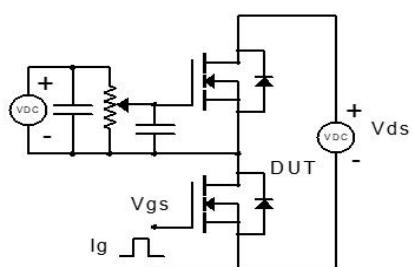


Figure 1: Gate Charge Test Circuit & Waveform

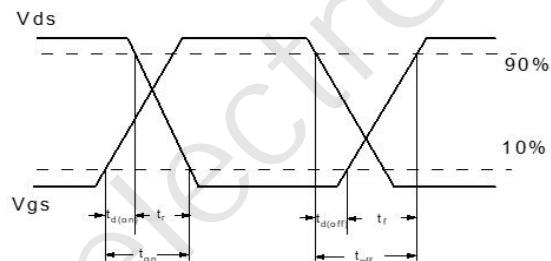
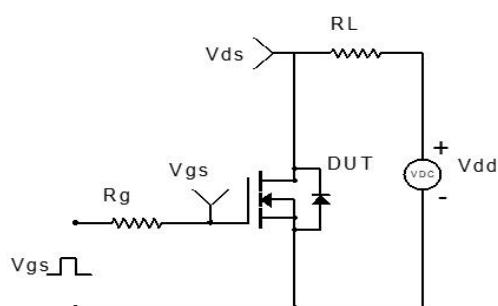


Figure 2: Resistive Switching Test Circuit & Waveform

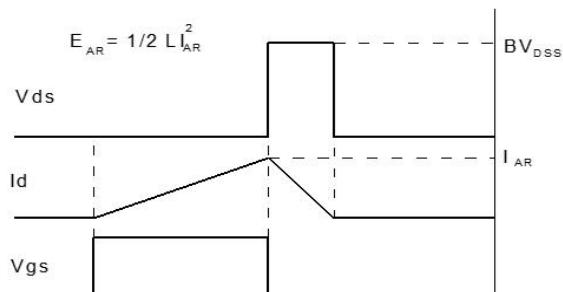
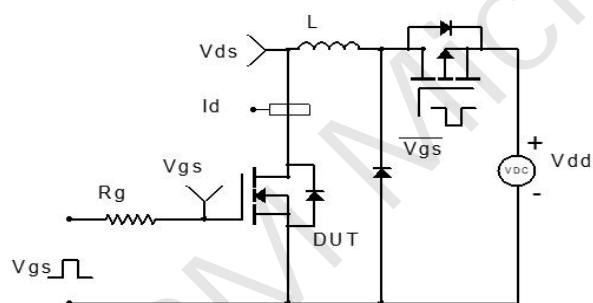


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

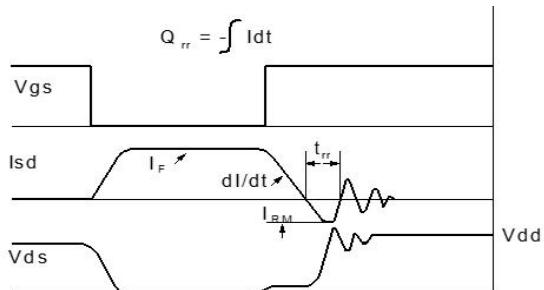
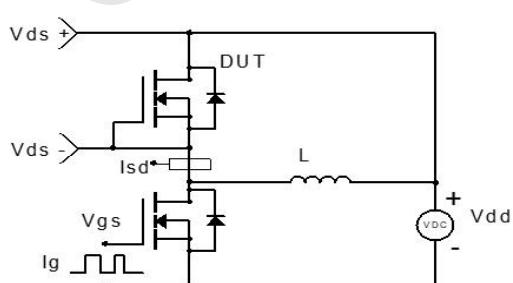
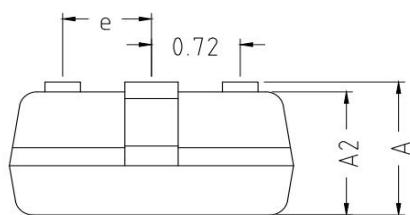
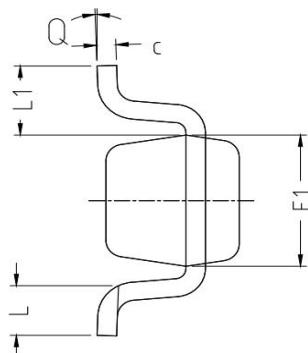
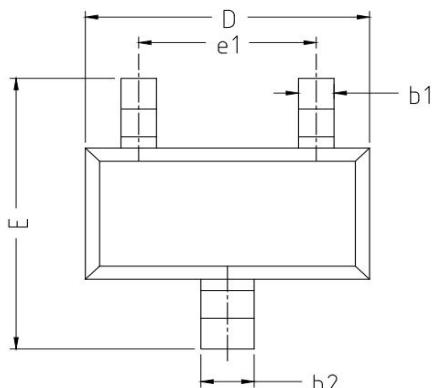


Figure 4: Diode Recovery Test Circuit & Waveform

### Package Mechanical Data(SOT-523-3L)



COMMON IN DIMENSION (MM)			
PKG	SOT-523		
Symbol	MIN	MON	MAX
A	0.700	0.800	0.900
A1	0.000	0.050	0.100
A2	0.700	0.750	0.800
b1	0.150	0.200	0.250
b2	0.250	0.300	0.350
c	0.100	0.130	0.200
D	1.550	1.600	1.700
E	1.450	1.600	1.750
E1	0.700	0.800	0.900
e	0.500 TYP		
e1	0.900	1.000	1.100
L	0.260	0.360	0.460
L1	0.400REF		
Q	0°	4°	8°

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