### **Description**

### **N-channel Enhancement Mode Power MOSFET**

#### **Features**

• 100V, 60A

 $R_{DS(ON)}$  Typ= 10m $\Omega$  @  $V_{GS}$  = 10V  $R_{DS(ON)}$  Typ= 13m $\Omega$  @  $V_{GS}$  = 4.5V

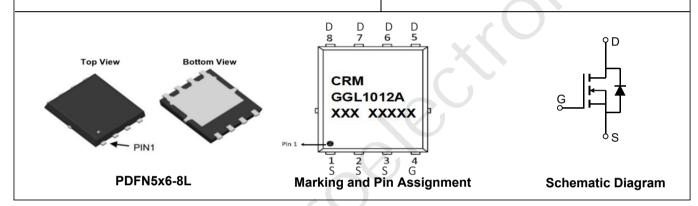
- Advanced Split Gate Trench Technology
- Excellent R<sub>DS(ON)</sub> and Low Gate Charge

#### **Applications**

- Load Switch
- PWM Application
- Power Management

100% UIS TESTED! 100% ΔVds TESTED!





#### **Package Marking and Ordering Information**

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
CRMGGL1012A	CRMGGL1012A	TAPING	PDFN5x6-8L	13"	5000	50000

#### Absolute Maximum Ratings (@ T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter		Value	Units	
V <sub>DS</sub>	Drain-to-Source Voltage		100	V	
V <sub>GS</sub>	Gate-to-Source Voltage		±20	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	60	А	
		T <sub>C</sub> = 100°C	36		
I <sub>DM</sub>	Pulsed Drain Current (1)		240	А	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (2)		64	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	78	W	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	°C/W	
T <sub>J</sub> , T <sub>STG</sub>	Junction & Storage Temperature Range		-55 to 150	°C	

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#### **Electrical Characteristics** (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	-	-	1.0	μА
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	ı	±100	nA
On Cha	racteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0	1.7	2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source ON-Resistance <sup>(3)</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A	-	10.0	13.0	mΩ
		$V_{GS} = 4.5V, I_D = 25A$	-	13.0	17.0	mΩ
Dynami	ic Characteristics					
C <sub>iss</sub>	Input Capacitance		- (	1500	-	pF
C <sub>oss</sub>	Output Capacitance	$V_{GS} = 0V, V_{DS} = 25V,$ f = 1MHz		840	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	30	-	pF
$Q_g$	Total Gate Charge	V 01 40V	_	35	-	nC
$Q_{gs}$	Gate Source Charge	$V_{GS} = 0 \text{ to } 10V$ $V_{DS} = 50V, I_{D} = 15A$	0	4.5	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 13A	-	8	-	nC
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On DelayTime		-	16	-	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10V, V_{DD} = 50V$ $I_{D} = 15A, R_{GEN} = 3\Omega$	-	13	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	37	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	17	-	ns
Drain-S	Source Diode Characteristics and N	lax Ratings				
I <sub>s</sub>	Maximum Continuous Drain to Source Diode Forward Current			-	60	А
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	240	Α
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{S} = 30A$	-	-	1.2	V

Notes:

<sup>1.</sup> Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

<sup>2.</sup>  $E_{AS}$  condition: Starting  $T_J$ =25C,  $V_{DD}$ =50V,  $V_G$ =10V,  $R_G$ =25ohm, L=0.5mH,  $I_{AS}$ =16A

<sup>3.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  0.5%.

## **Typical Performance Characteristics**

Figure 1: Output Characteristics

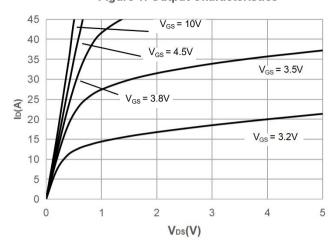


Figure 2: Typical Transfer Characteristics

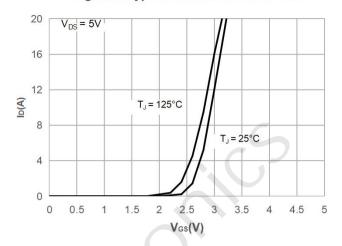


Figure 3: On-resistance vs. Drain Current

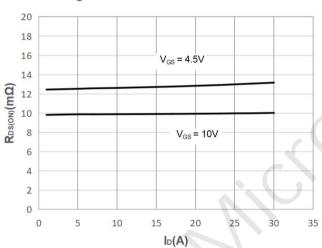


Figure 4: Body Diode Characteristics

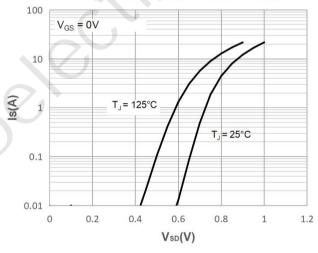


Figure 5: Gate Charge Characteristics

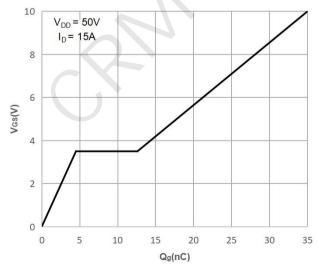
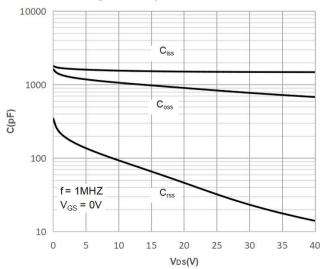


Figure 6: Capacitance Characteristics







## **Typical Performance Characteristics**

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

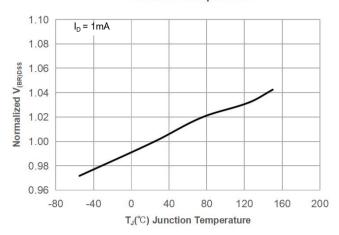


Figure 9: Maximum Safe Operating Area

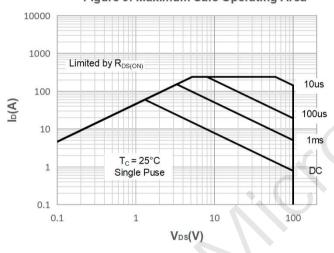


Figure 11: Normalized Maximum Transient Thermal Impedance

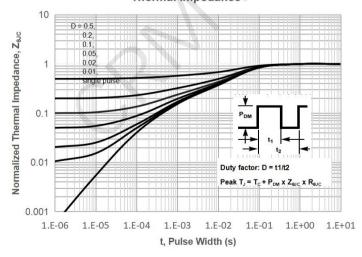


Figure 8: Normalized on Resistance vs. Junction Temperature

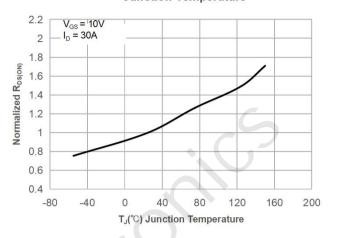


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

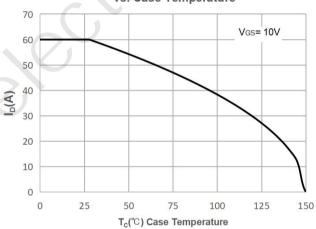
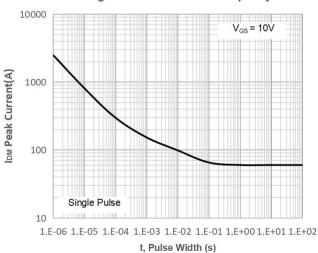


Figure 12: Peak Current Capacity





#### **Test Circuit**

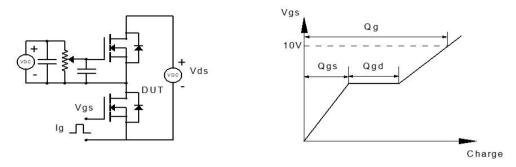


Figure 1: Gate Charge Test Circuit & Waveform

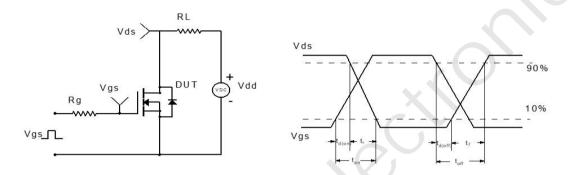


Figure 2: Resistive Switching Test Circuit & Waveform

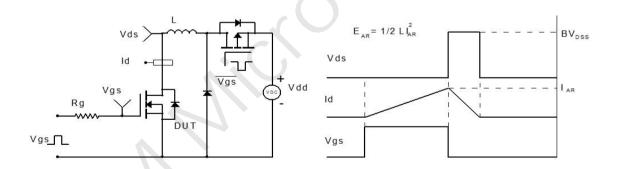


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

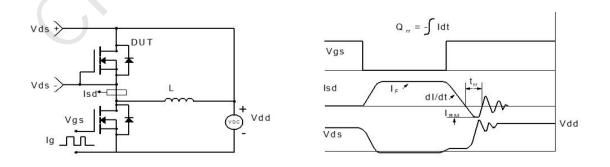
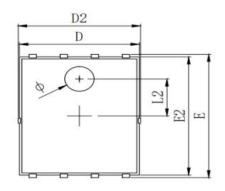
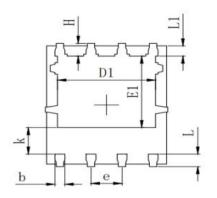


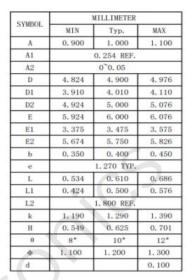
Figure 4: Diode Recovery Test Circuit & Waveform

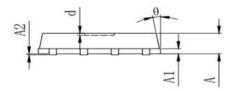


## Package Mechanical Data(PDFN5X6-8L)









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