

Description

N-channel Enhancement Mode Power MOSFET

Features

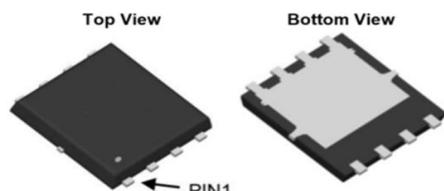
- 60V, 90A
- $R_{DS(ON)}$ Typ= 4.2mΩ @ V_{GS} = 10V
- $R_{DS(ON)}$ Typ= 5.8mΩ @ V_{GS} = 4.5V
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

Applications

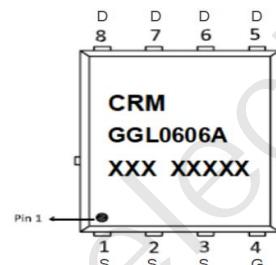
- Load Switch
- PWM Application
- Power Management



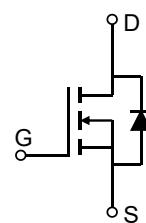
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN5x6-8L



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
CRMGGL0606A	CRMGGL0606A	TAPING	PDFN5x6-8L	13"	5000	50000

Absolute Maximum Ratings (@ T_J = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ\text{C}$	90	A
		55	
I_{DM}	Pulsed Drain Current ⁽¹⁾	360	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	121	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		$^\circ\text{C/W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.2	1.8	2.5	V
$R_{DS(\text{ON})}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	4.2	5.5	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	-	5.8	7.5	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	2140	-	pF
C_{oss}	Output Capacitance		-	850	-	pF
C_{rss}	Reverse Transfer Capacitance		-	60	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 30\text{V}, I_D = 20\text{A}$	-	30	-	nC
Q_{gs}	Gate Source Charge		-	4.5	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	5	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}$ $I_D = 20\text{A}, R_{\text{GEN}} = 6\Omega$	-	6.5	-	ns
t_r	Turn-On Rise Time		-	8	-	ns
$t_{d(\text{off})}$	Turn-Off DelayTime		-	38	-	ns
t_f	Turn-Off Fall Time		-	16	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	90	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	360	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_s = 30\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A/us}$	-	39	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	45	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=30\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=0.5\text{mH}$, $I_{AS}=22\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

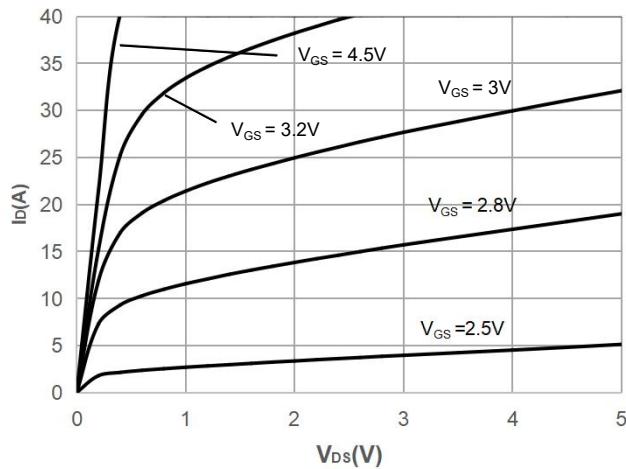


Figure 2: Typical Transfer Characteristics

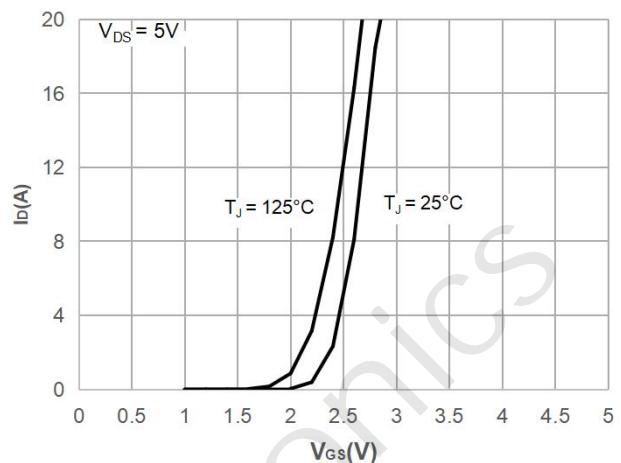


Figure 3: On-resistance vs. Drain Current

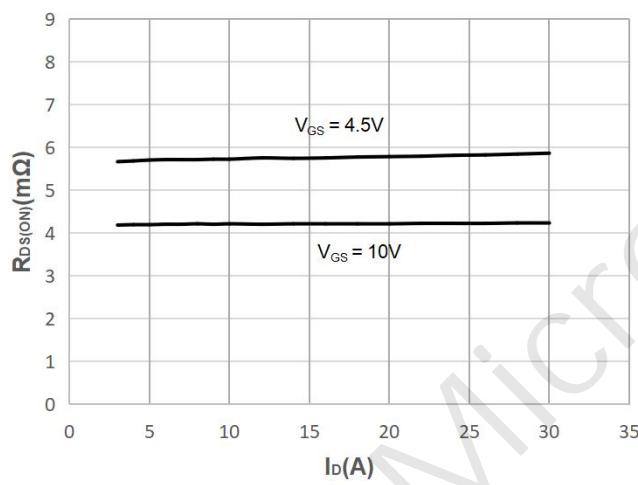


Figure 4: Body Diode Characteristics

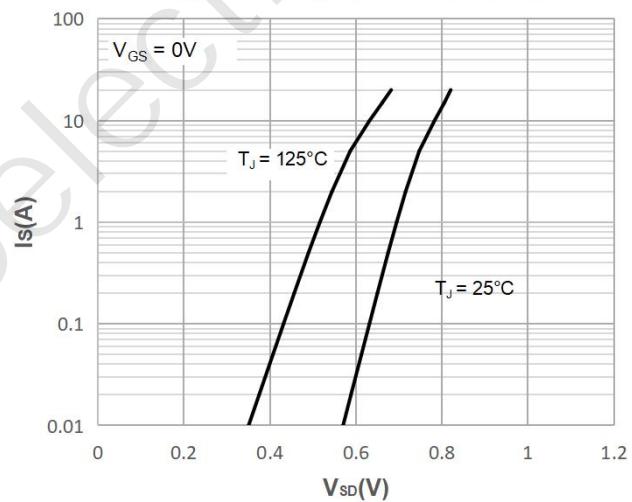


Figure 5: Gate Charge Characteristics

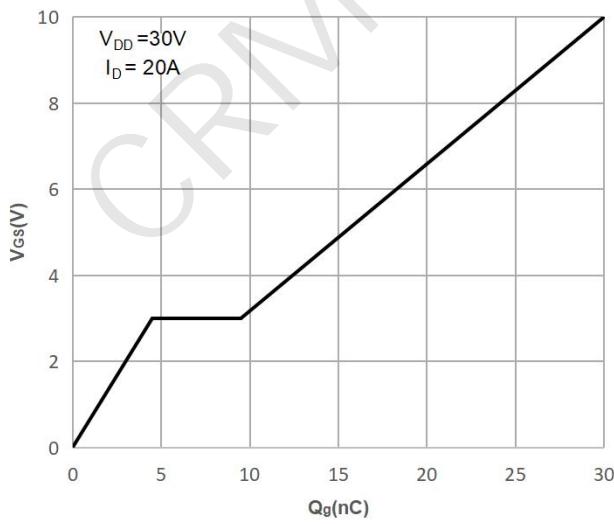
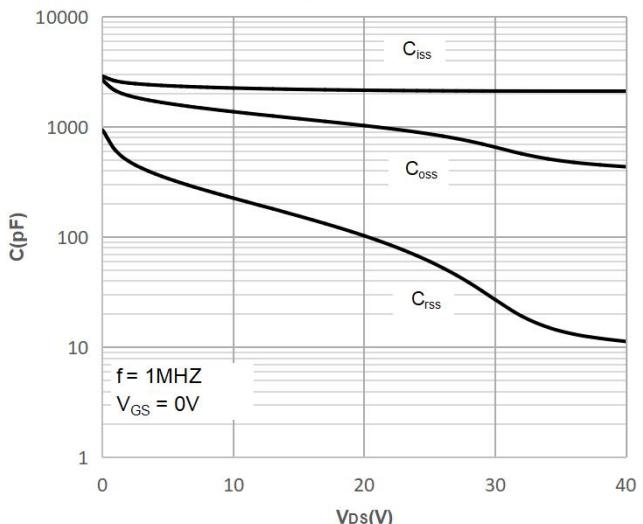


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

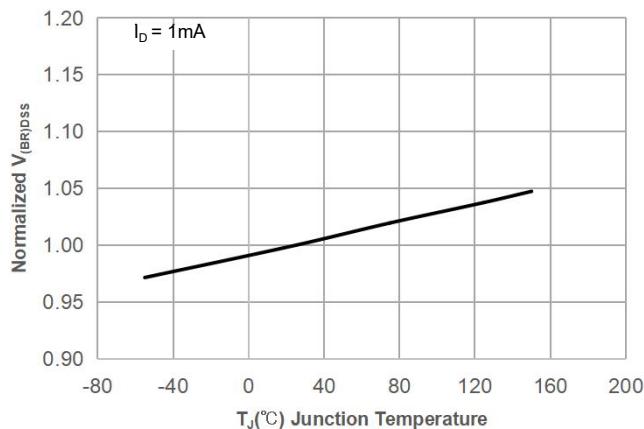


Figure 8: Normalized on Resistance vs. Junction Temperature

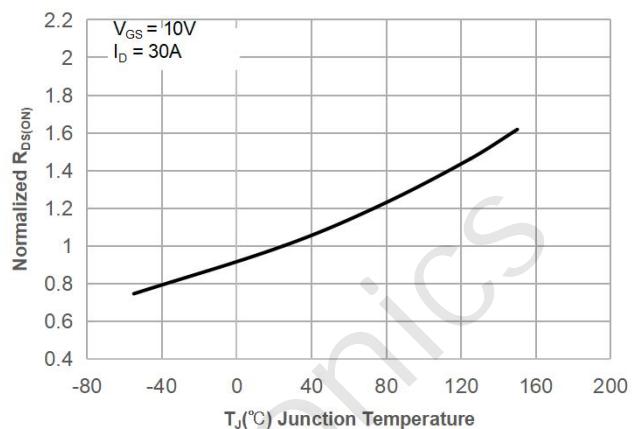


Figure 9: Maximum Safe Operating Area

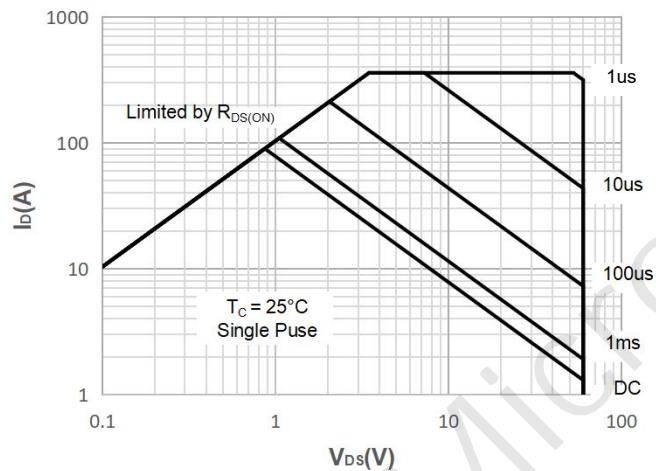


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

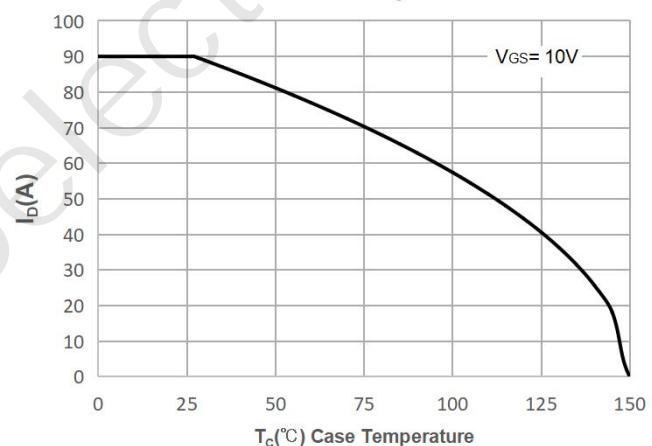


Figure 11: Normalized Maximum Transient Thermal Impedance

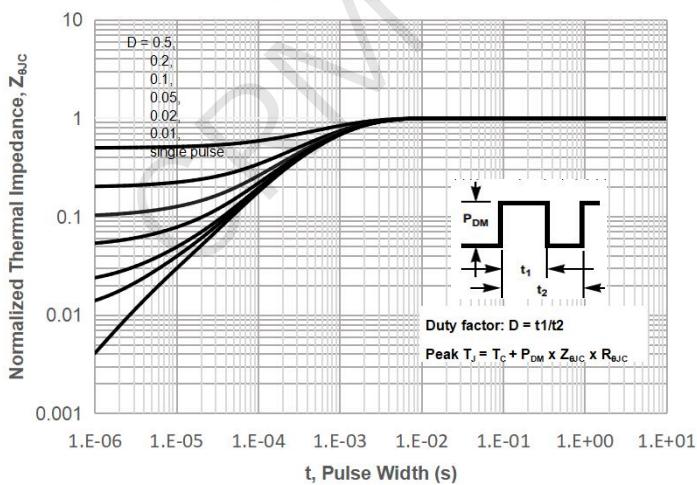
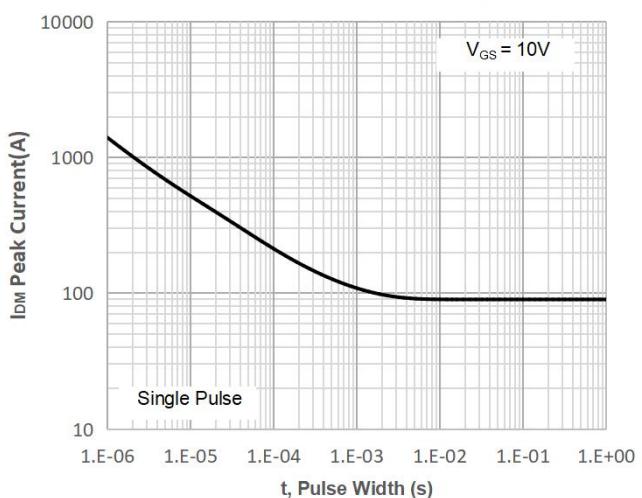


Figure 12: Peak Current Capacity



Test Circuit

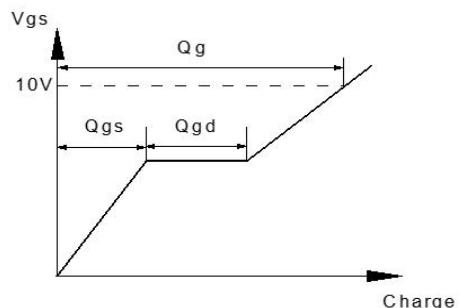
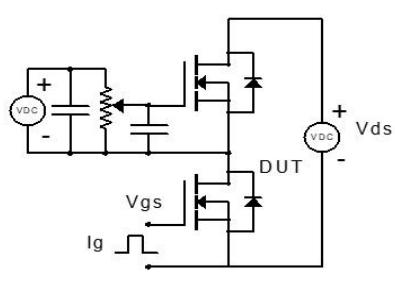


Figure 1: Gate Charge Test Circuit & Waveform

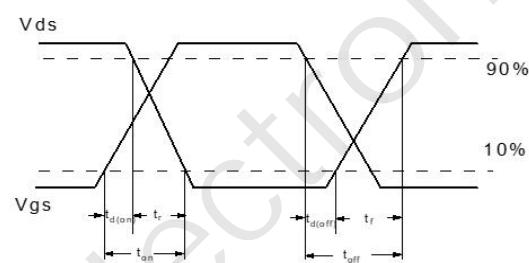
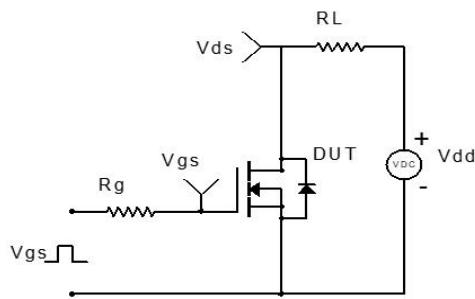


Figure 2: Resistive Switching Test Circuit & Waveform

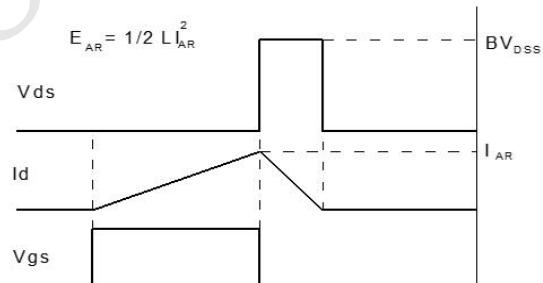
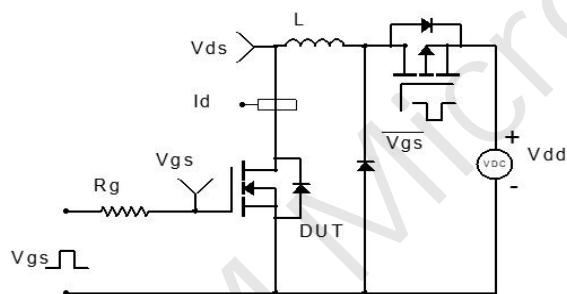


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

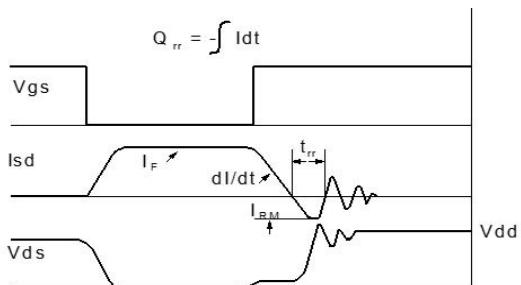
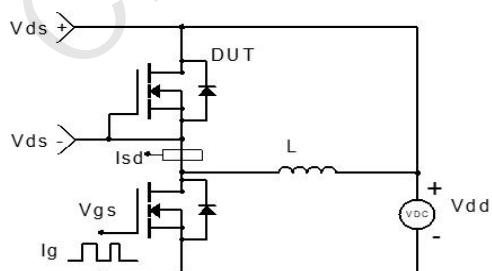
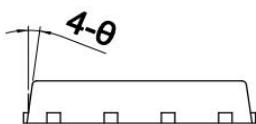
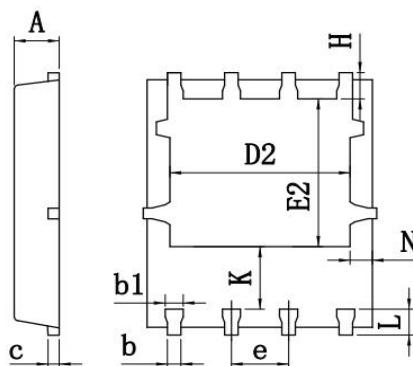
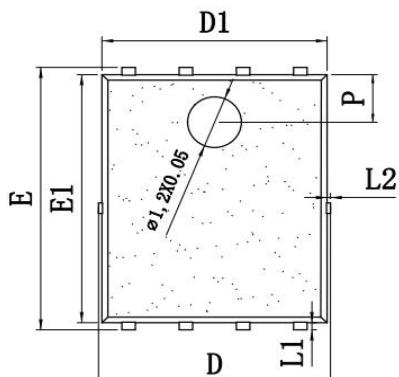


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN5X6-8L)



SYMBOL	mm		
	MIN	NOM	MAX
*A	0.95	1.00	1.05
*b	0.25	0.30	0.35
*b1	0.30	0.40	0.50
*c	0.20	0.25	0.30
D	5.15BSC		
*D1	4.90	5.00	5.10
D2	3.90	4.01	4.20
*e	1.17	1.27	1.37
E	6.15BSC		
*E1	5.75	5.85	5.95
E2	3.35	3.50	3.65
H	0.51	0.61	0.71
K	1.10	1.35	1.50
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2	-	-	0.12
N	0.40	0.50	0.60
P	0.95	1.10	1.25
θ	9°	11°	13°

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