

Description

N-channel Enhancement Mode Power MOSFET

Features

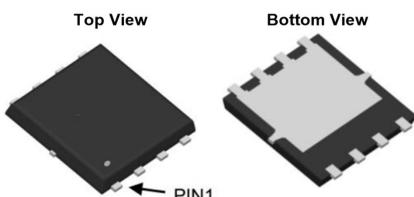
- 60V, 15A
- $R_{DS(ON)} < 37m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} < 45m\Omega$ @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management



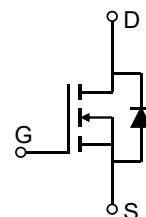
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3.3x3.3-8L



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
CRMQTL0637A	CRMQTL0637A	TAPING	PDFN3.3x3.3-8L	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ C$	15	A
		9	
I_{DM}	Pulsed Drain Current ⁽¹⁾	60	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	25	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		$^\circ C/W$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.1	1.6	2.1	V
$R_{DS(\text{ON})}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	-	28.0	37.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$	-	34.0	45.0	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	860	-	pF
C_{oss}	Output Capacitance		-	62	-	pF
C_{rss}	Reverse Transfer Capacitance		-	51	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 30\text{V}, I_D = 10\text{A}$	-	20.3	-	nC
Q_{gs}	Gate Source Charge		-	3.7	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	5.3	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}$ $I_D = 5\text{A}, R_{\text{GEN}} = 1.8\Omega$	-	6	-	ns
t_r	Turn-On Rise Time		-	6	-	ns
$t_{d(\text{off})}$	Turn-Off DelayTime		-	19	-	ns
t_f	Turn-Off Fall Time		-	3	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	15	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_s = 10\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 5\text{A}, di/dt = 100\text{A/us}$	-	13	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	9	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=30\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=0.5\text{mH}$, $I_{AS}=10\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Test Circuit

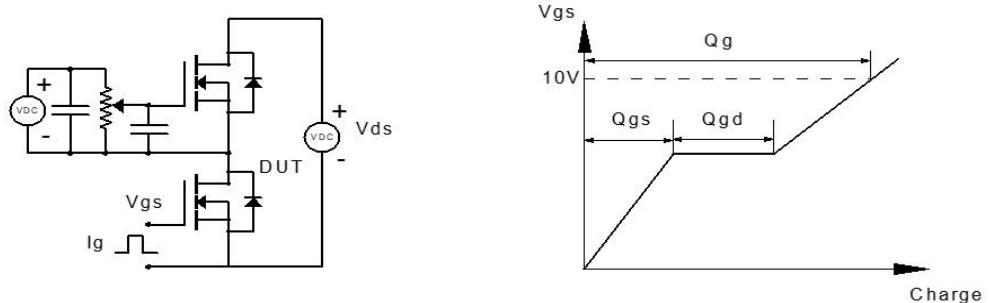


Figure 1: Gate Charge Test Circuit & Waveform

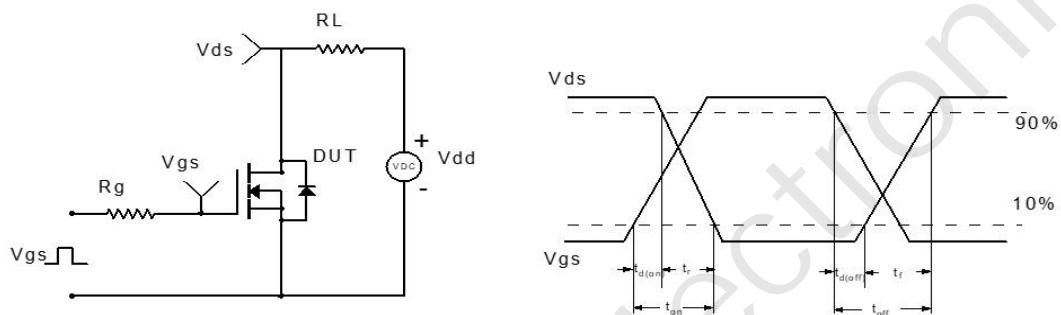


Figure 2: Resistive Switching Test Circuit & Waveform

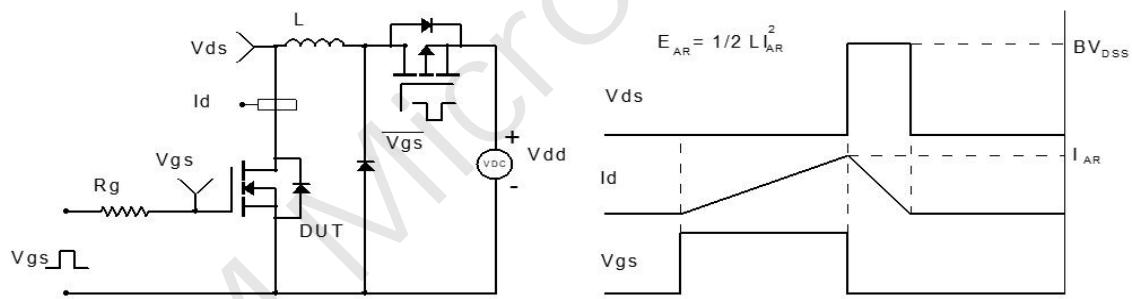


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

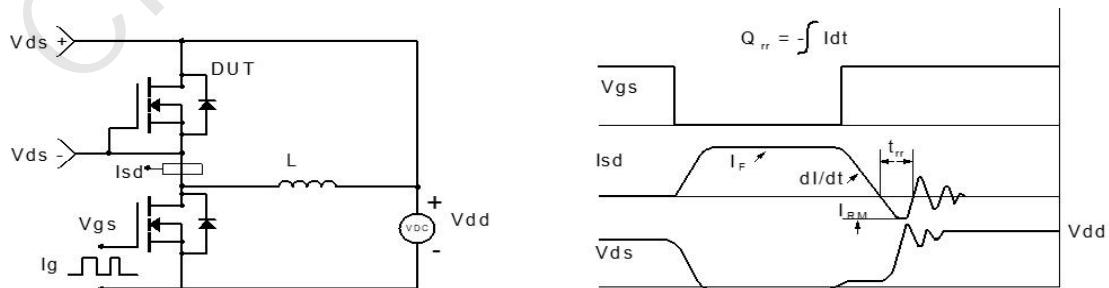
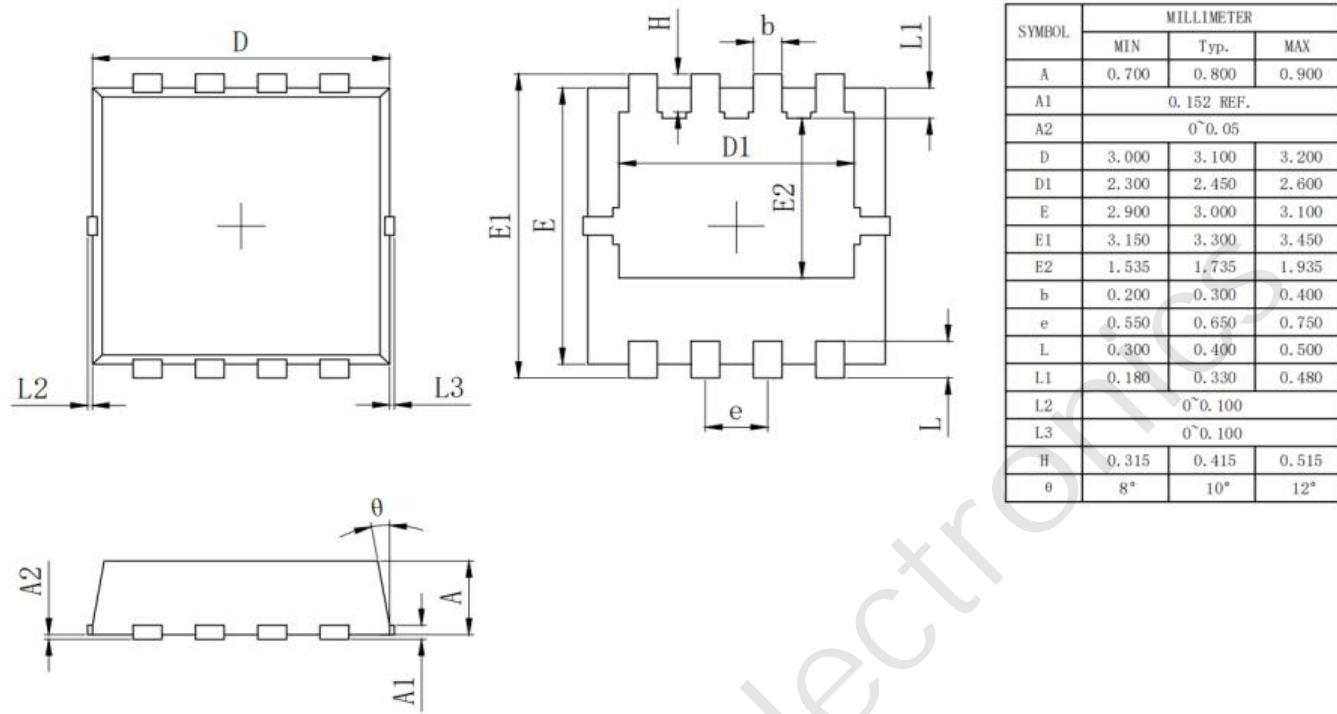


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN3.3x3.3-8L)



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