



Description

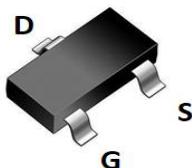
N-channel Enhancement Mode Power MOSFET

Features

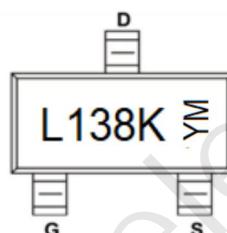
- 60V, 0.2A
- $R_{DS(ON)} < 2.2\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} < 3\Omega$ @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free
- ESD Protected: 2KV

Applications

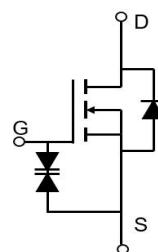
- Battery Operated System
- Direct logic-level Interface: TTL/CMOS
- Solid-State Relays



SOT-323-3L



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
L138K	CRMLATL138K	TAPING	SOT-323-3L	7"	3000	120000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ C$	0.2	A
		0.13	
I_{DM}	Pulsed Drain Current ⁽¹⁾	0.8	A
P_D	Power Dissipation $T_C = 25^\circ C$	0.3	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	415	$^\circ C/W$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 10	μA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.7	1.1	1.5	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS} = 10\text{V}, I_D = 0.3\text{A}$	-	1.8	2.2	Ω
		$V_{GS} = 4.5\text{V}, I_D = 0.2\text{A}$	-	2.0	3.0	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	22	-	pF
C_{oss}	Output Capacitance		-	3.4	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.3	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 4.5\text{V}$ $V_{DS} = 10\text{V}, I_D = 0.3\text{A}$	-	1.6	-	nC
Q_{gs}	Gate Source Charge		-	0.2	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	0.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 10\text{V}$ $I_D = 0.2\text{A}, R_{\text{GEN}} = 10\Omega$	-	2	-	ns
t_r	Turn-On Rise Time		-	14	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	6	-	ns
t_f	Turn-Off Fall Time		-	19	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	0.3	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	1.2	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_s = 0.3\text{A}$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Test Circuit

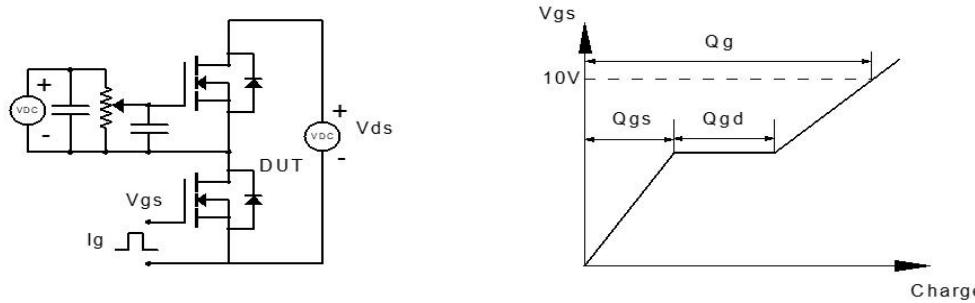


Figure 1: Gate Charge Test Circuit & Waveform

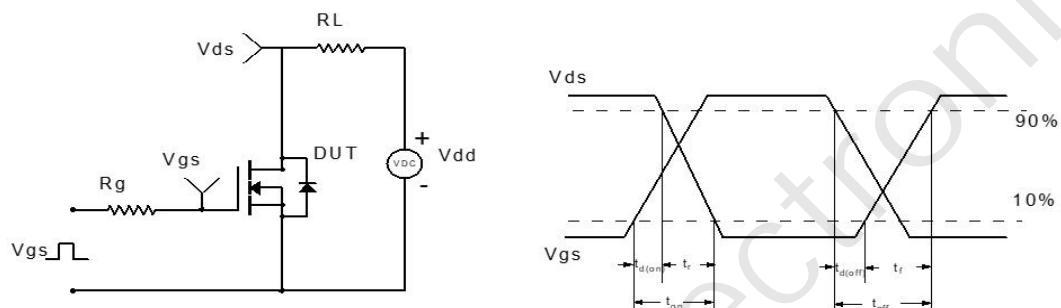


Figure 2: Resistive Switching Test Circuit & Waveform

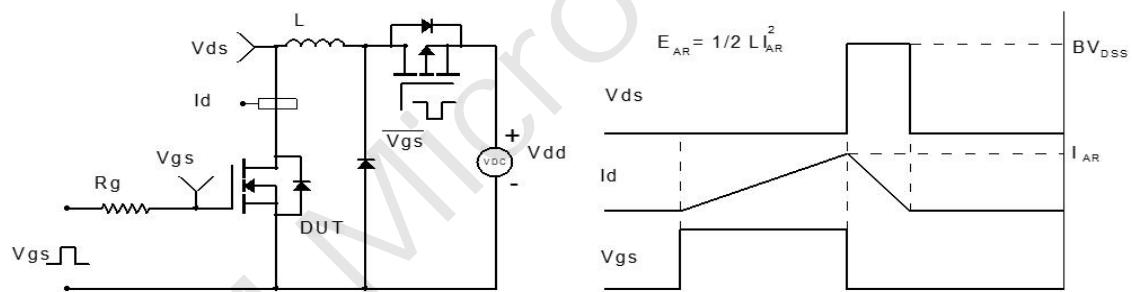


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

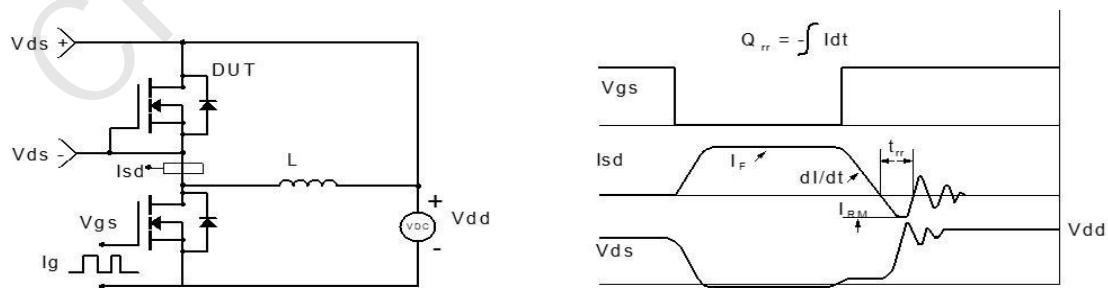
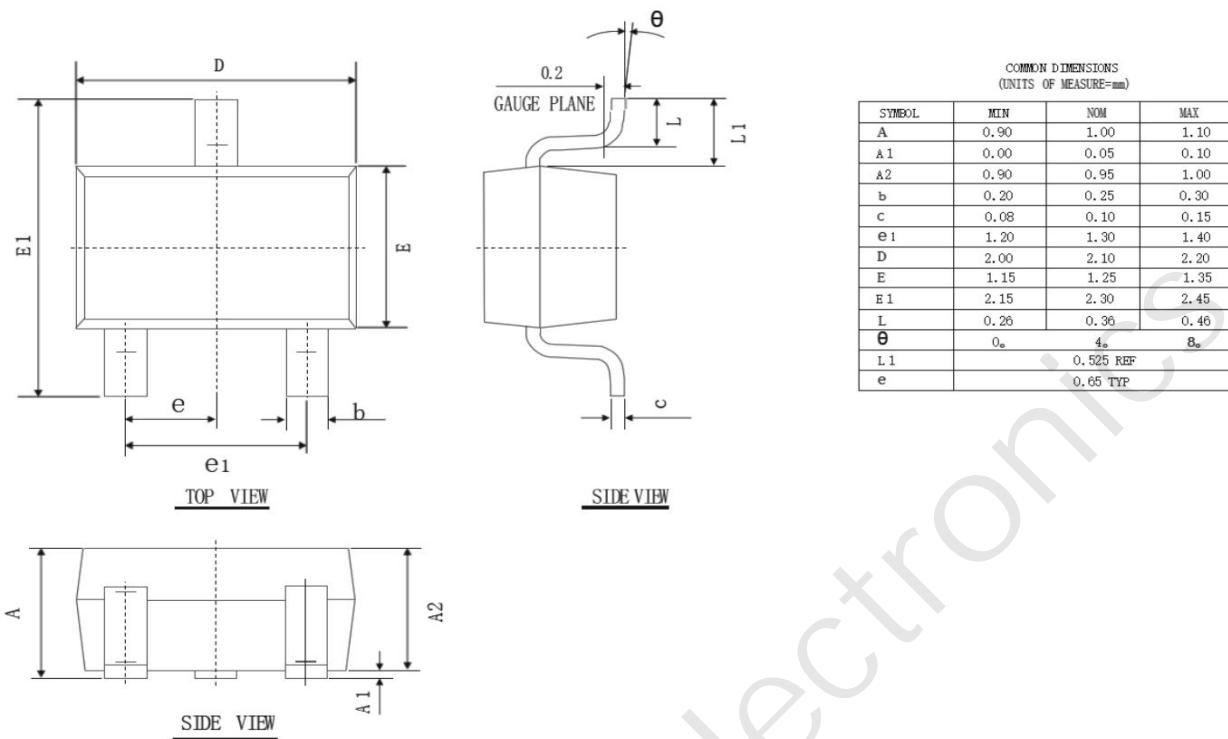


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOT-323-3L)



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