

Description

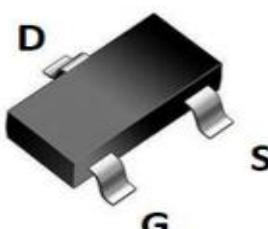
N-channel Enhancement Mode Power MOSFET

Features

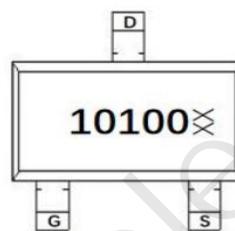
- 100V, 3A
- $R_{DS(ON)} < 115\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 127\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

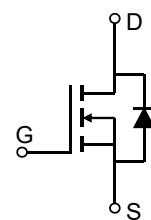
- Load Switch
- PWM Application
- Power Management



SOT-23-3L



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
10100	CRMJTL10120A	TAPING	SOT-23-3L	7"	3000	120000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ\text{C}$	3	A
		2	
I_{DM}	Pulsed Drain Current ⁽¹⁾	12	A
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	90	$^\circ\text{C/W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.5	2.5	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽²⁾	$V_{GS} = 10\text{V}, I_D = 3\text{A}$	-	92.0	115.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 2\text{A}$	-	98.0	127.0	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	847	-	pF
C_{oss}	Output Capacitance		-	40	-	pF
C_{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 50\text{V}, I_D = 2\text{A}$	-	20	-	nC
Q_{gs}	Gate Source Charge		-	2.8	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	4	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 50\text{V}$ $I_D = 3\text{A}, R_{\text{GEN}} = 1.8\Omega$	-	6	-	ns
t_r	Turn-On Rise Time		-	7	-	ns
$t_{d(\text{off})}$	Turn-Off DelayTime		-	21	-	ns
t_f	Turn-Off Fall Time		-	3	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	3	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	12	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 3\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 3\text{A}, di/dt = 100\text{A/us}$	-	15	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

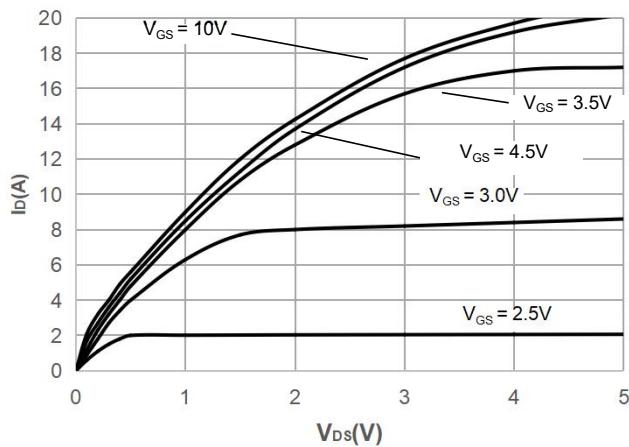


Figure 2: Typical Transfer Characteristics

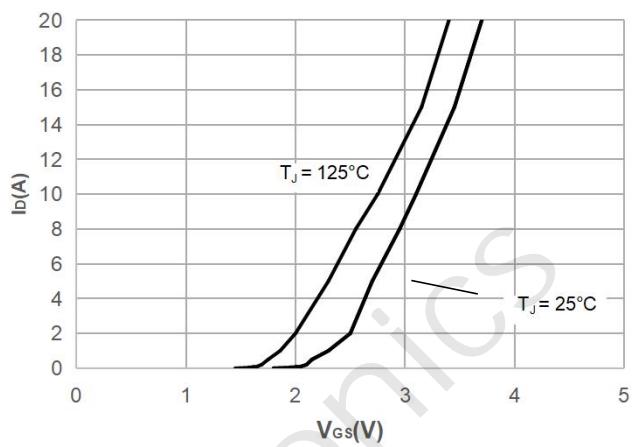


Figure 3: On-resistance vs. Drain Current

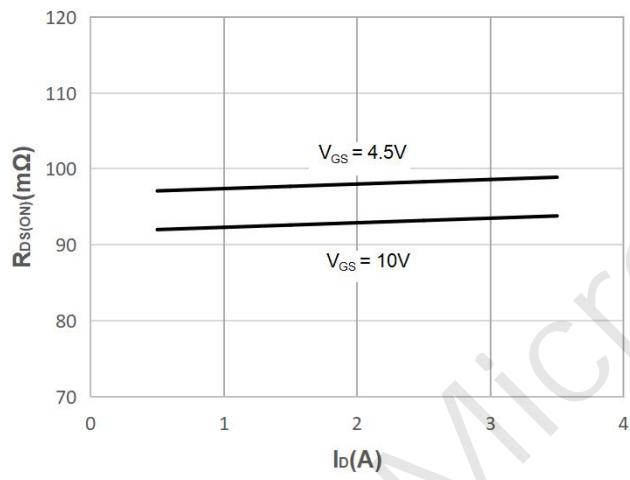


Figure 4: Body Diode Characteristics

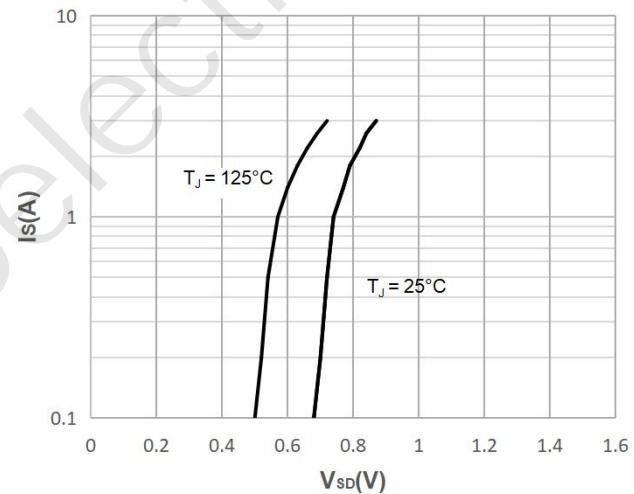


Figure 5: Gate Charge Characteristics

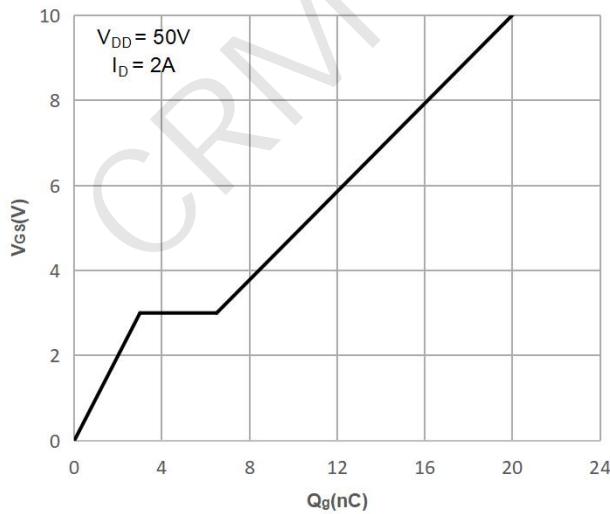
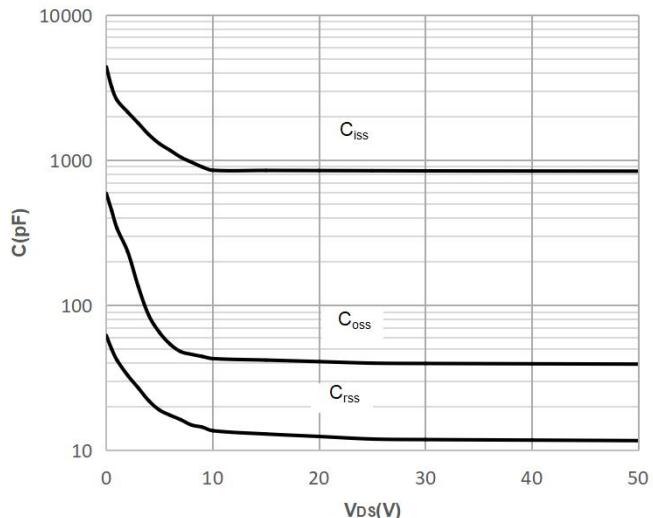


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

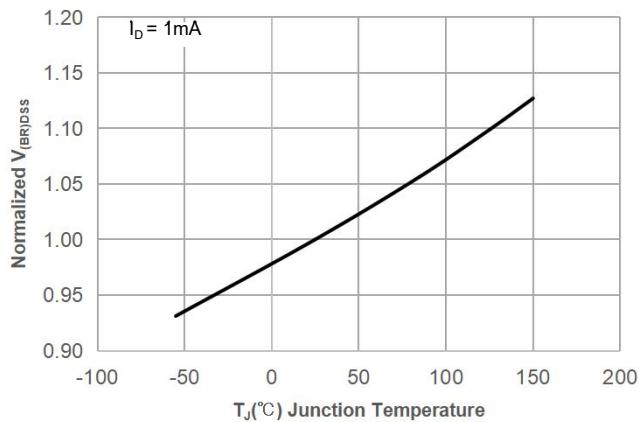


Figure 8: Normalized on Resistance vs. Junction Temperature

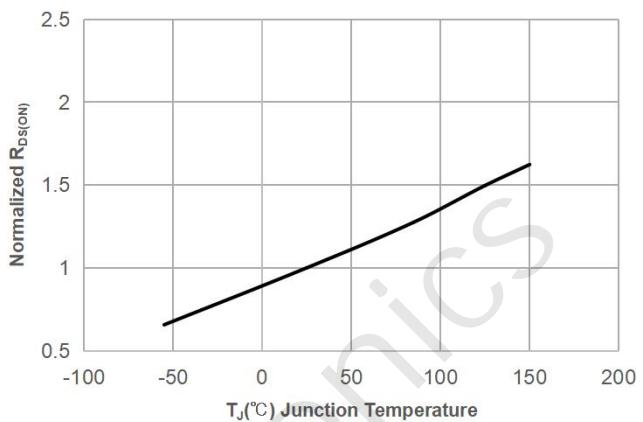


Figure 9: Maximum Safe Operating Area

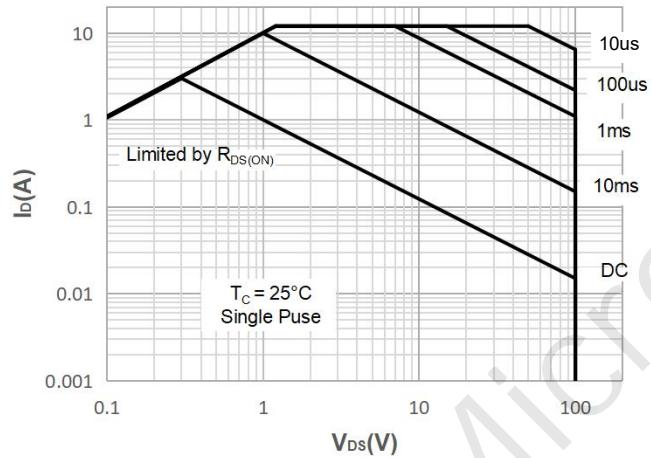


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

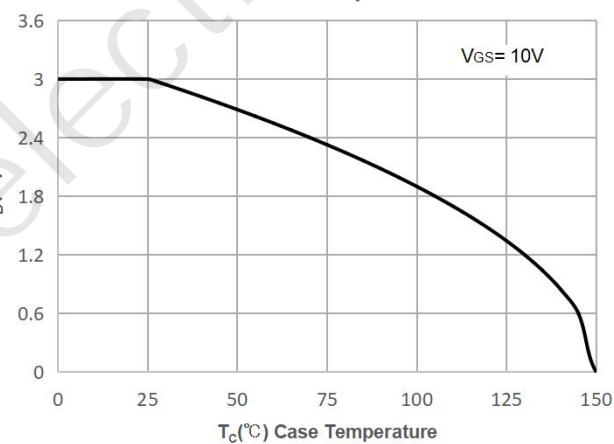


Figure 11: Normalized Maximum Transient Thermal Impedance

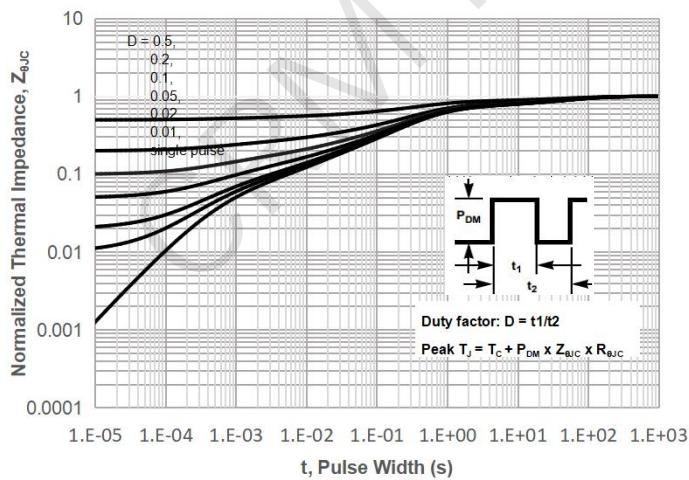
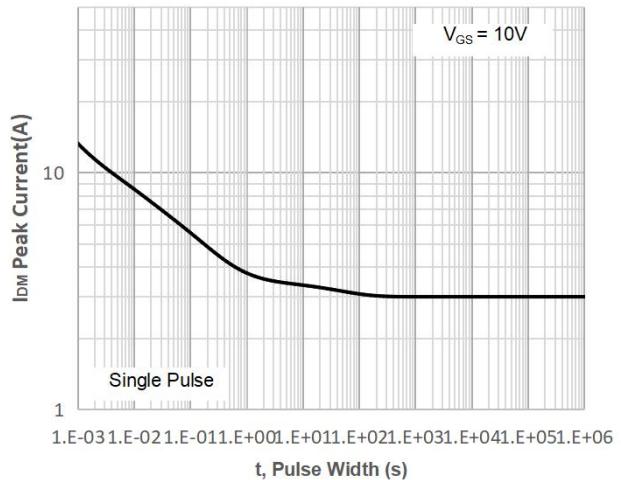


Figure 12: Peak Current Capacity



Test Circuit

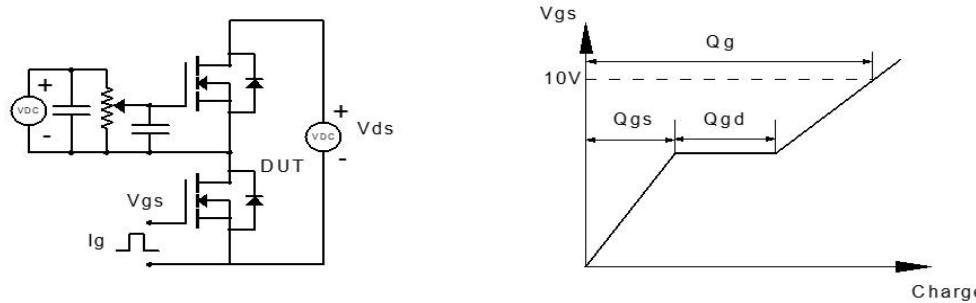


Figure 1: Gate Charge Test Circuit & Waveform

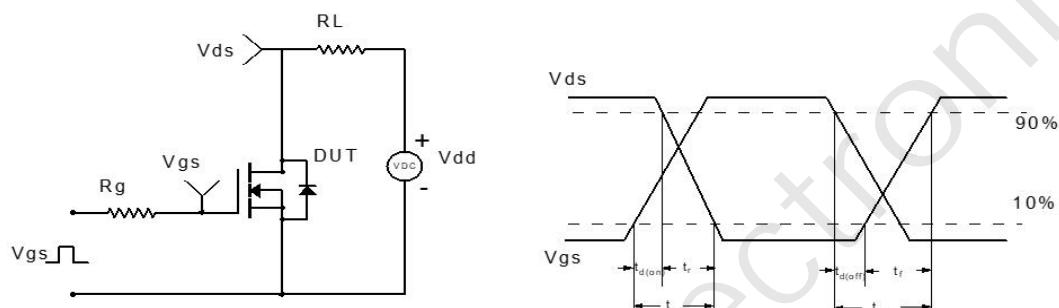


Figure 2: Resistive Switching Test Circuit & Waveform

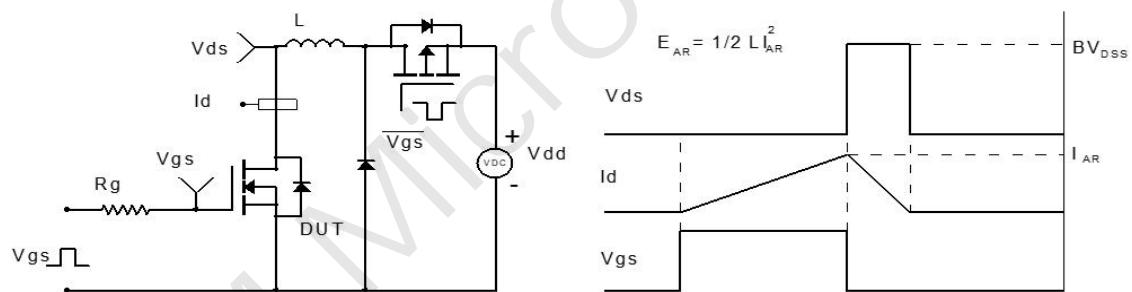


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

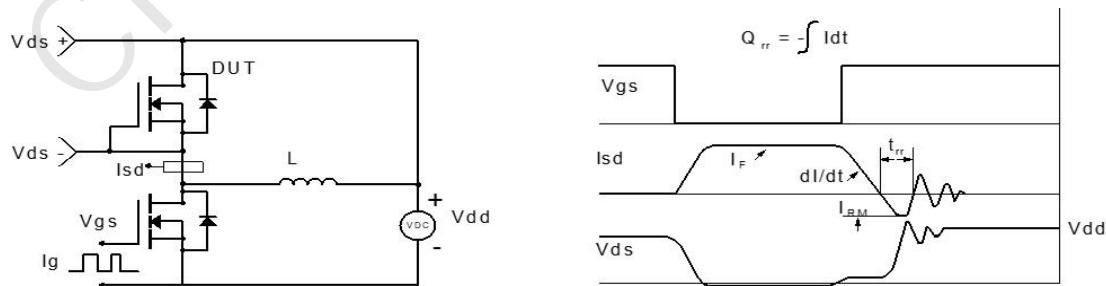
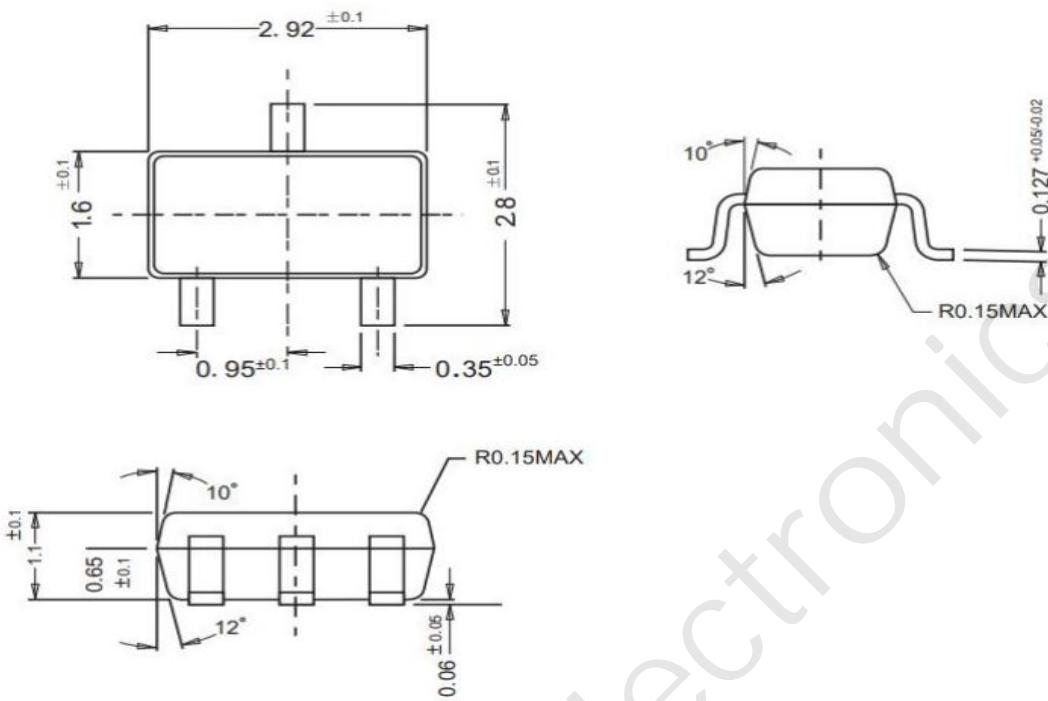


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOT-23-3L)



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